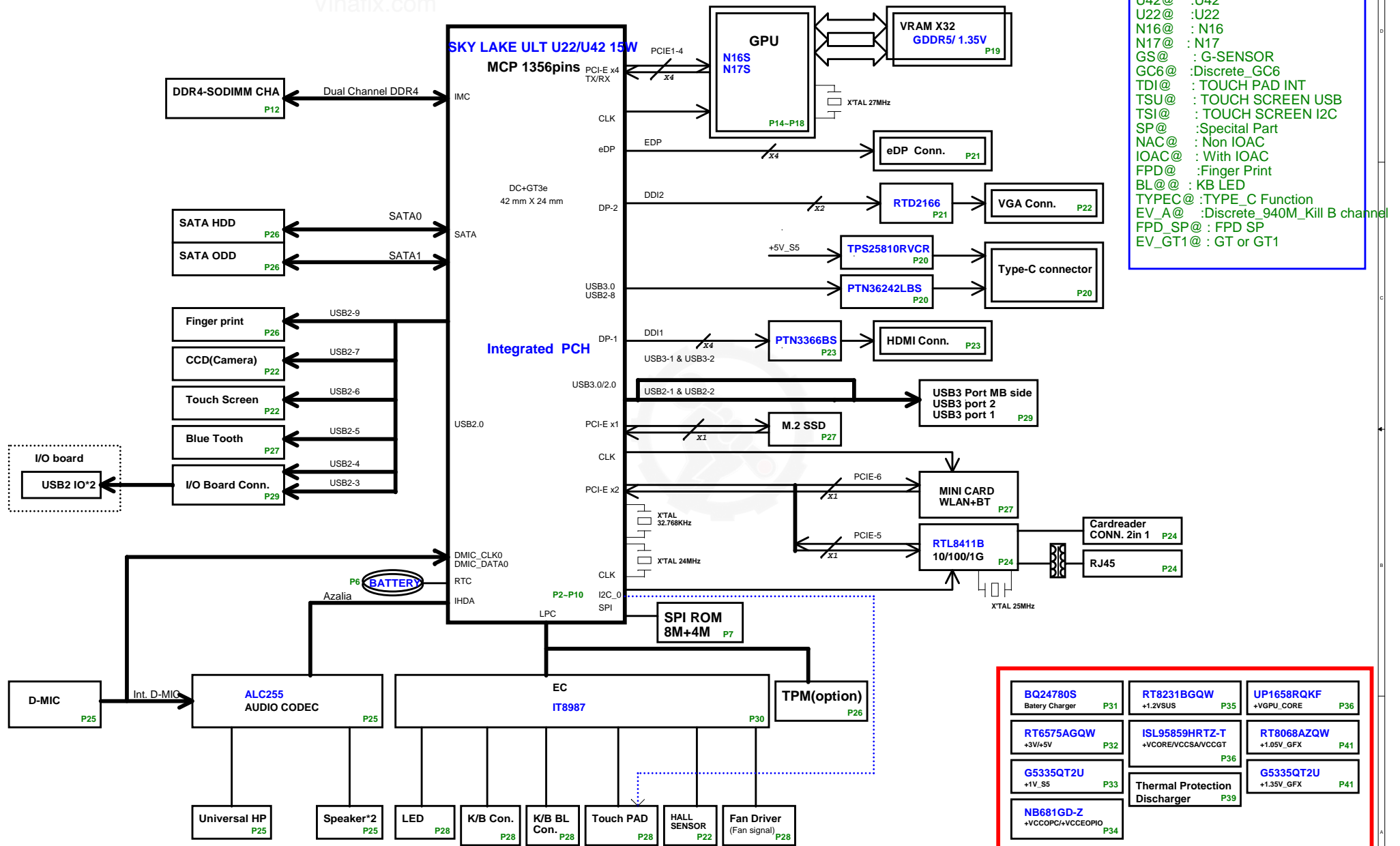
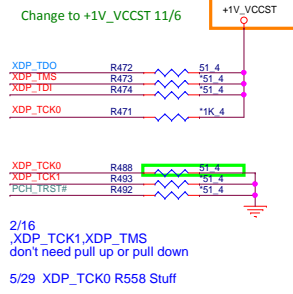
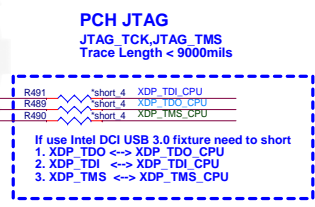
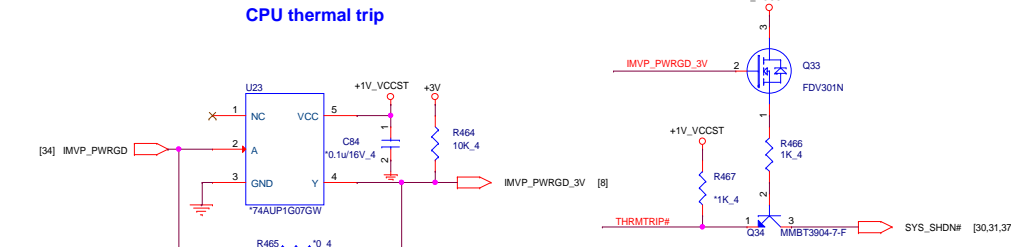
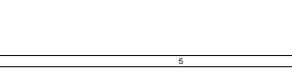
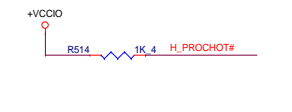
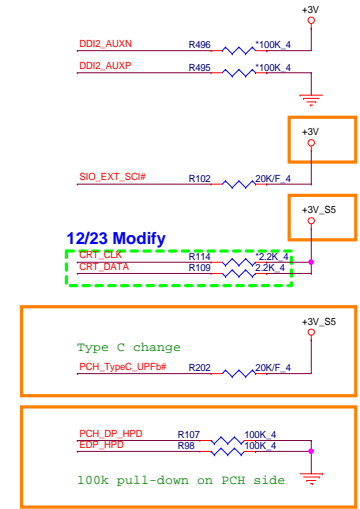
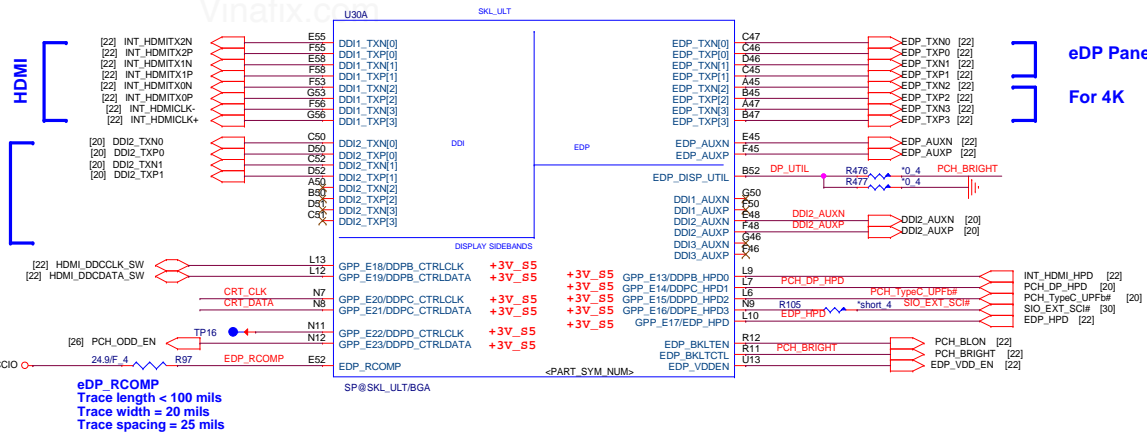


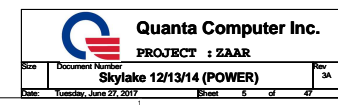
ZAAR Serials SkyLake-U SYSTEM BLOCK DIAGRAM

Vinafix.com



SkyLake ULT (DISPLAY,eDP)





Skylake ULT (GPU, SATA , ODD, CLK ,USB2&3)

+3V [2,4,7,8,9,12,13,14,15,16,17,20,22,23,25,26,27,28,30,31,32,33,34,37,38,39,40]
 +3V_S5 [2,3,4,7,8,9,11,20,23,25,27,28,30,31,33,39]
 +3VPCU [9,11,22,23,25,26,27,28,30,31,37,40]
 +3V_RTC [8,9,30]
 +1V_S5 [9,32]

dGPU PEG#4

For Thunderbolt

LAN

WIFI

For M.2 SSD -NA

For M.2 SSD -1

Rev:D change to shortpad

Rev:D add for EC reset RTC

Rev:E Reserve only

1V power plane
0.71 checklist p14

MB USB3.0 (Charger IC)

MB USB3.0

For TYPE-C

MB USB3.0 (Charger IC)

MB USB3.0

DB USB2.0

For 17" DB use

BT

Touch Screen

CCD

For TYPE-C

POA

USBCOMP
Impedance = 50 ohm
Trace length < 500 mils
Trace spacing = 15 mils

MB U3
MB U3
DB U2
TYPE C

Green CPU

PCH PU/PD

USB_OC0# R80 10K 4
 USB_OC1# R77 10K 4
 USB_OC2# R46 10K 4
 USB_OC3# R494 10K 4

SATA_DEVSLP0 R548 10K 4
 SATA_DEVSLP1 R554 10K 4
 SATA_DEVSLP2 R551 10K 4
 PIRQAF R692 10K 4

SATAGP1 R546 10K 4

Add SSD ID 1/4

High is SSD, Low is ODD

[26] SSD_ID R547 10K 4 SATAGP0 R555 100K 4

Skylake-U used 24 MHz (50 Ohm ESR) XTAL

24MHz: BG624000078
 38.4MHz: ?

Note: Change Y4 to 38.4 MHz(ESR 30 ohm) for Cannonlake U

RTC Clock 32.768KHz (RTC)

Trace length < 1000 mils

CH01006JB08 -> 10p
 CH01506JB06 -> 15p
 CH-6806TB01 -> 6.8p

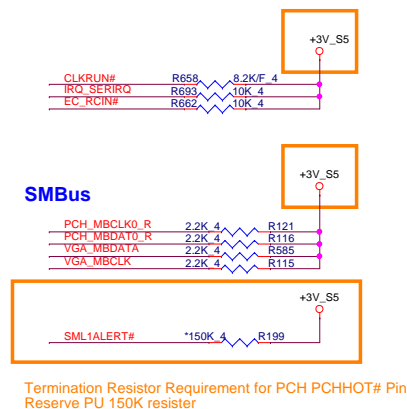
BG332768453 -> SEG
 BG332768104 -> TXC
 ZAA 2nd BG332768111

RTC Circuitry (RTC)

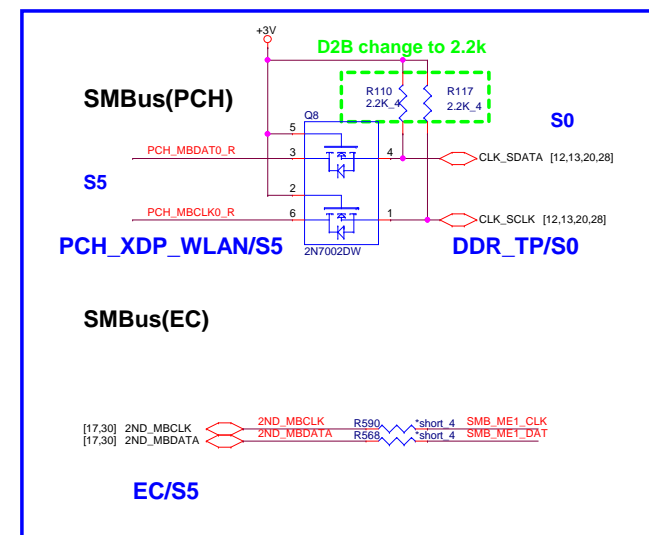
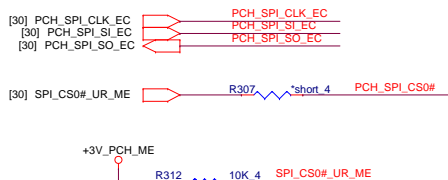
On SKL voltage at VCCRTC does not exceed 3.2V

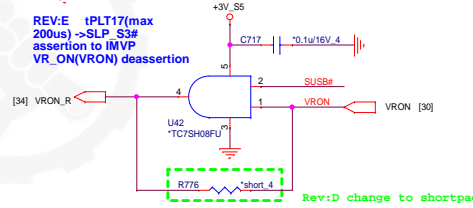
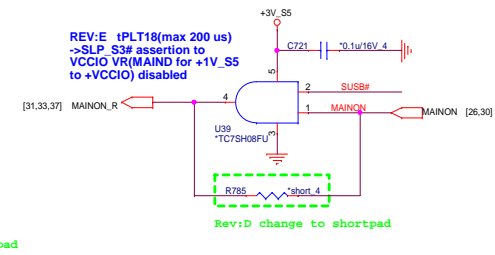
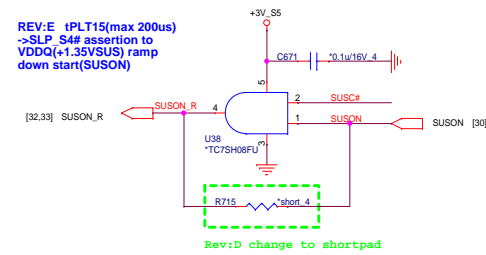
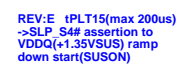
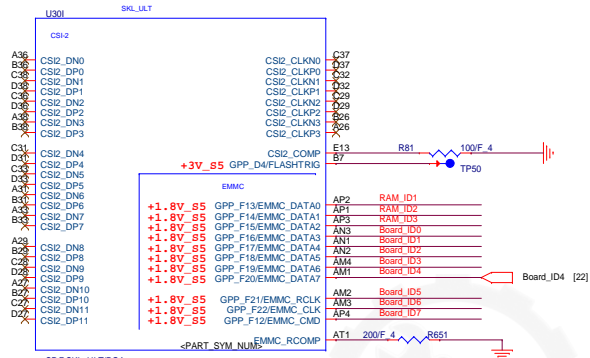
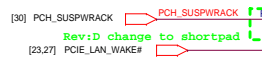
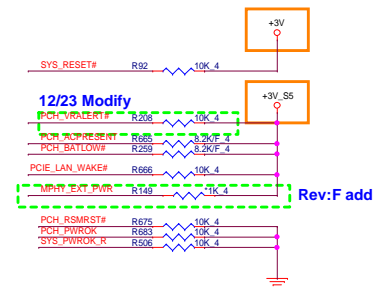
+3VPCU
 R344 1.5K 4
 R343 45.3K 4
 VCCRTC 2
 R342 1K 4 +3V_RTC_1
 BAT1
 BAT_CONN
 1A-22013/10/16 Charge +3V_RTC_0 to VCCRTC_2

1. AHL03003057 DBV CR2032
2. AHL03003003 VDE CR2032



SPI ROM	Vender	Size	Quanta P/N	Vender P/N
Skylake 3.3V	WND	8M	AKE3EFPN07	W25Q64FVSSIQ
	GGD	8M	AKE2EZNOQ00	GD25B64CSIGR





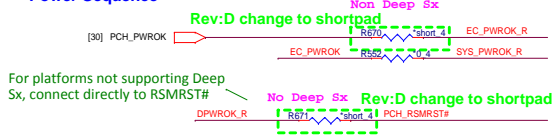
Board ID

Pin	Signal	Pin	Signal
R644	U22@10K_4	R645	U42@10K_4
R646	U4@10K_4	R647	U4@10K_4
R648	U4@10K_4	R649	U4@10K_4
R650	U4@10K_4	R651	U4@10K_4
R652	U4@10K_4	R653	U4@10K_4
R654	U4@10K_4	R655	U4@10K_4
R656	U4@10K_4	R657	U4@10K_4
R164	U4@10K_4	R165	U4@10K_4
R166	U4@10K_4	R167	U4@10K_4
R168	EV_GT1@10K_4	R169	U4@10K_4
R170	U4@10K_4	R171	U4@10K_4
R172	U4@10K_4	R173	U4@10K_4
R174	U4@10K_4	R175	U4@10K_4
R176	U4@10K_4	R177	U4@10K_4

+1.9V_S5

Default U42 stuff R639 & unstuff R638 for ZAA8

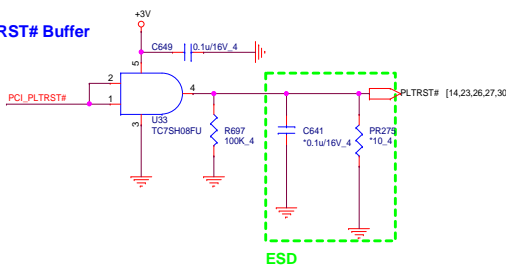
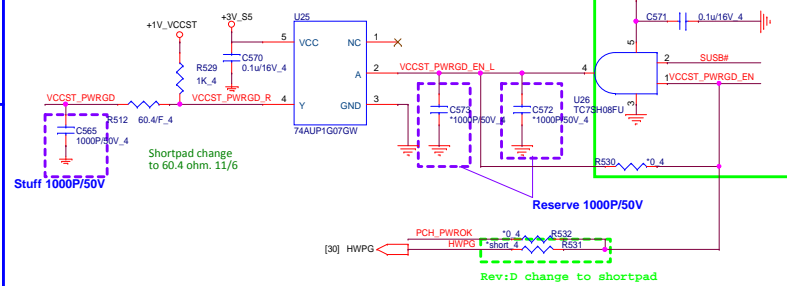
Power Sequence



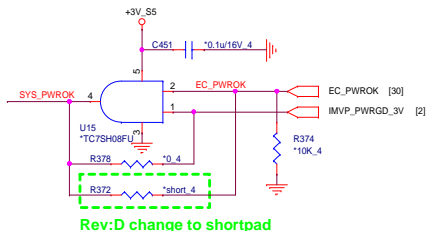
For platforms not supporting Deep
Sy, connect directly to BSMRST#

g Deep
RST# — No Deep Sx Rev:D change to shortpad

VCCST PWRGD CRB is via +1.05V PG

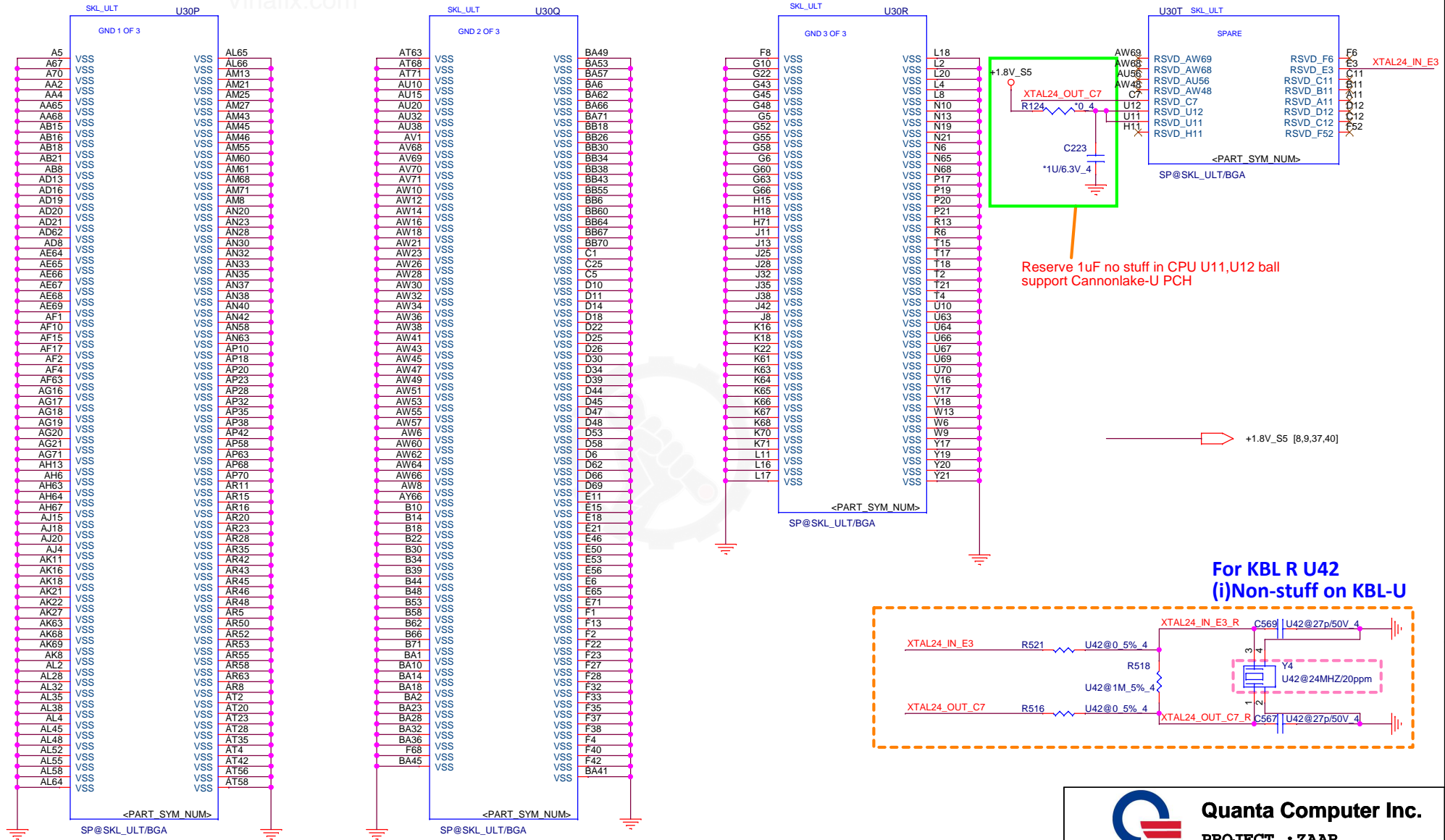


SYSPWOK



Skylake ULT (GND)

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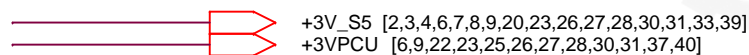
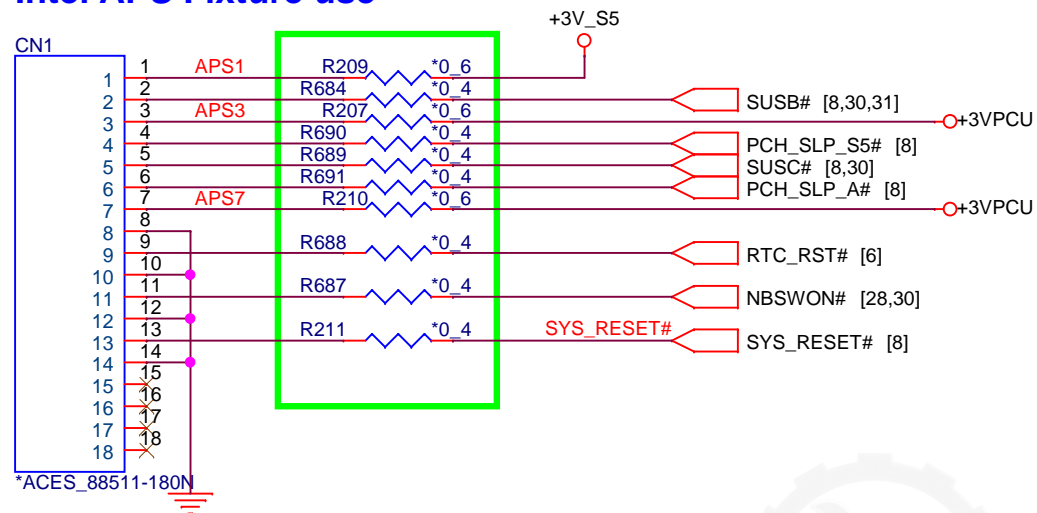


Quanta Computer Inc.

PROJECT : ZAAR

Size	Document Number	Rev
	Skylake 10/17/18 (GND)	3A
Date:	Friday, June 23, 2017	Sheet 10 of 47

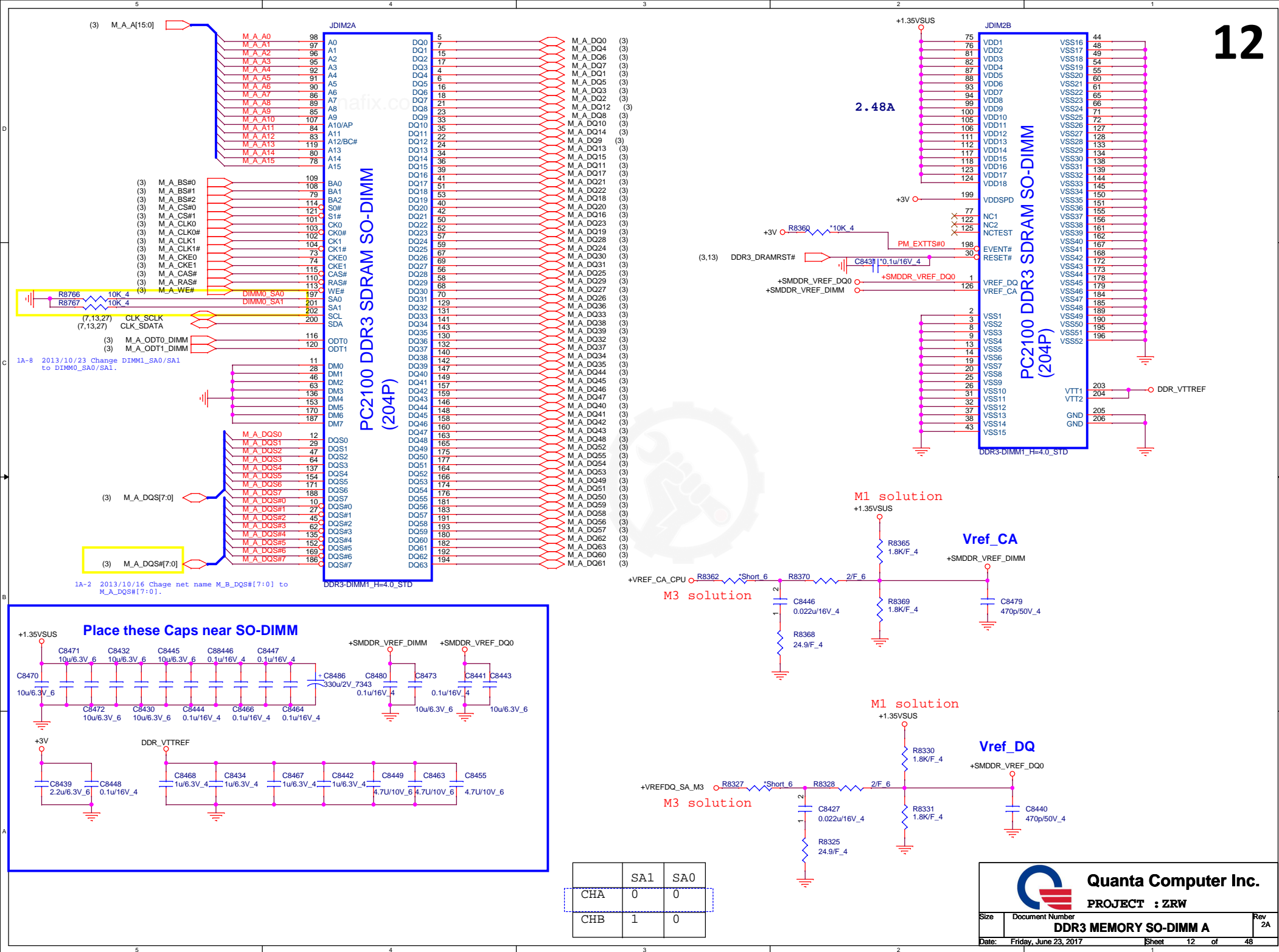
Intel APS Fixture use

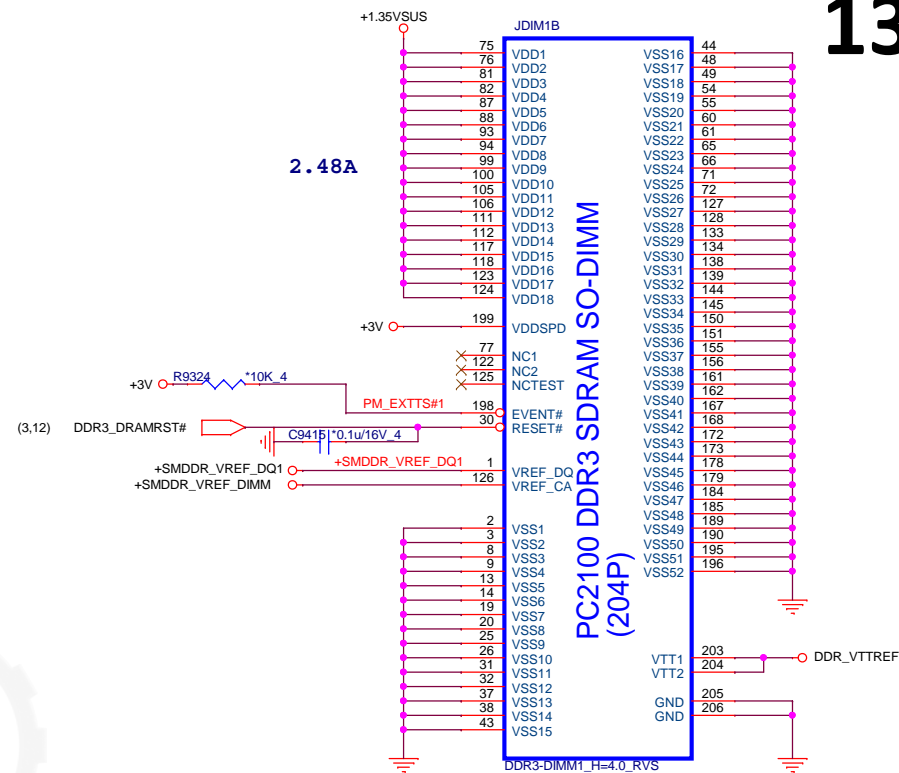
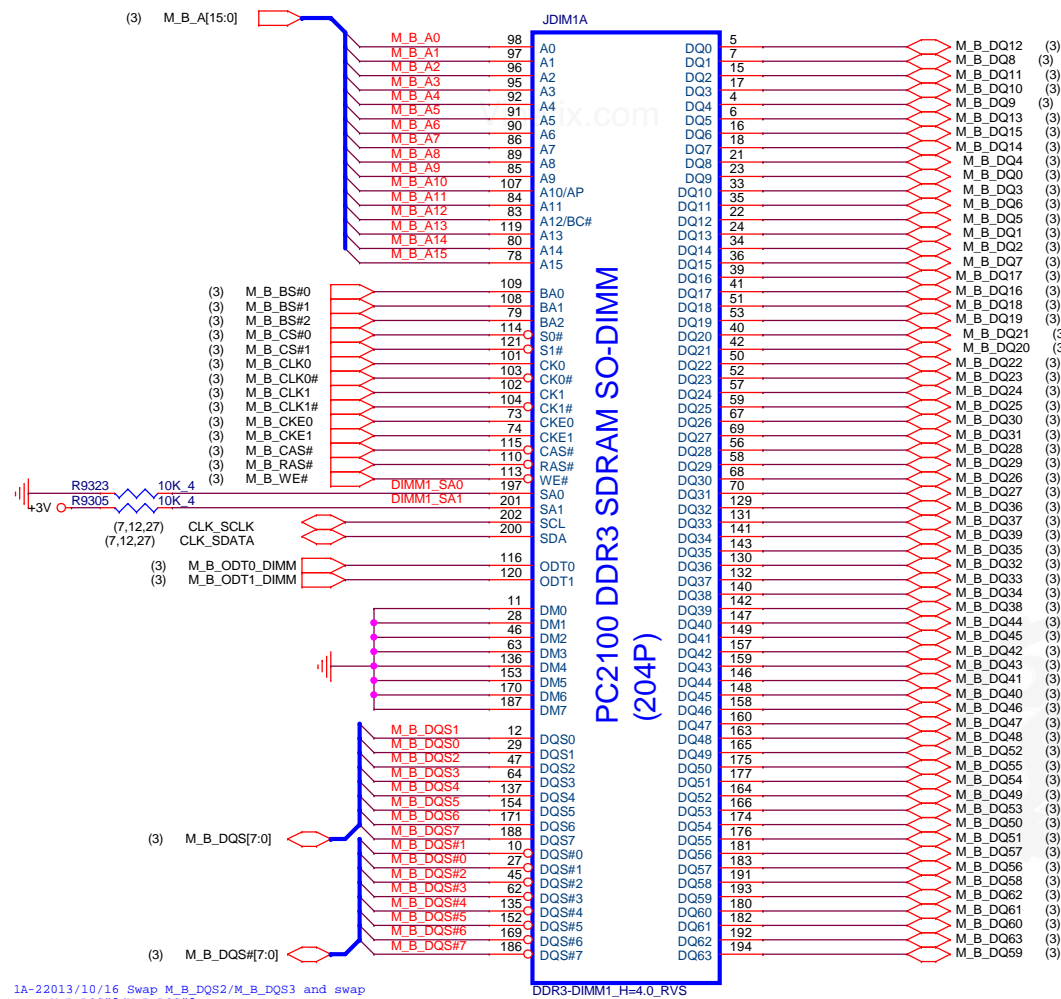


Quanta Computer Inc.

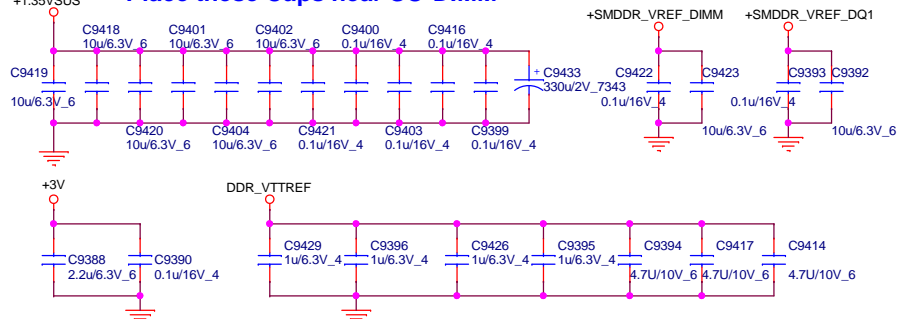
PROJECT : ZAAR

Size	Document Number	Rev
	CPU/PCH XDP	3A
Date:	Friday, June 23, 2017	Sheet 11 of 47





Place these Caps near SO-DIMM

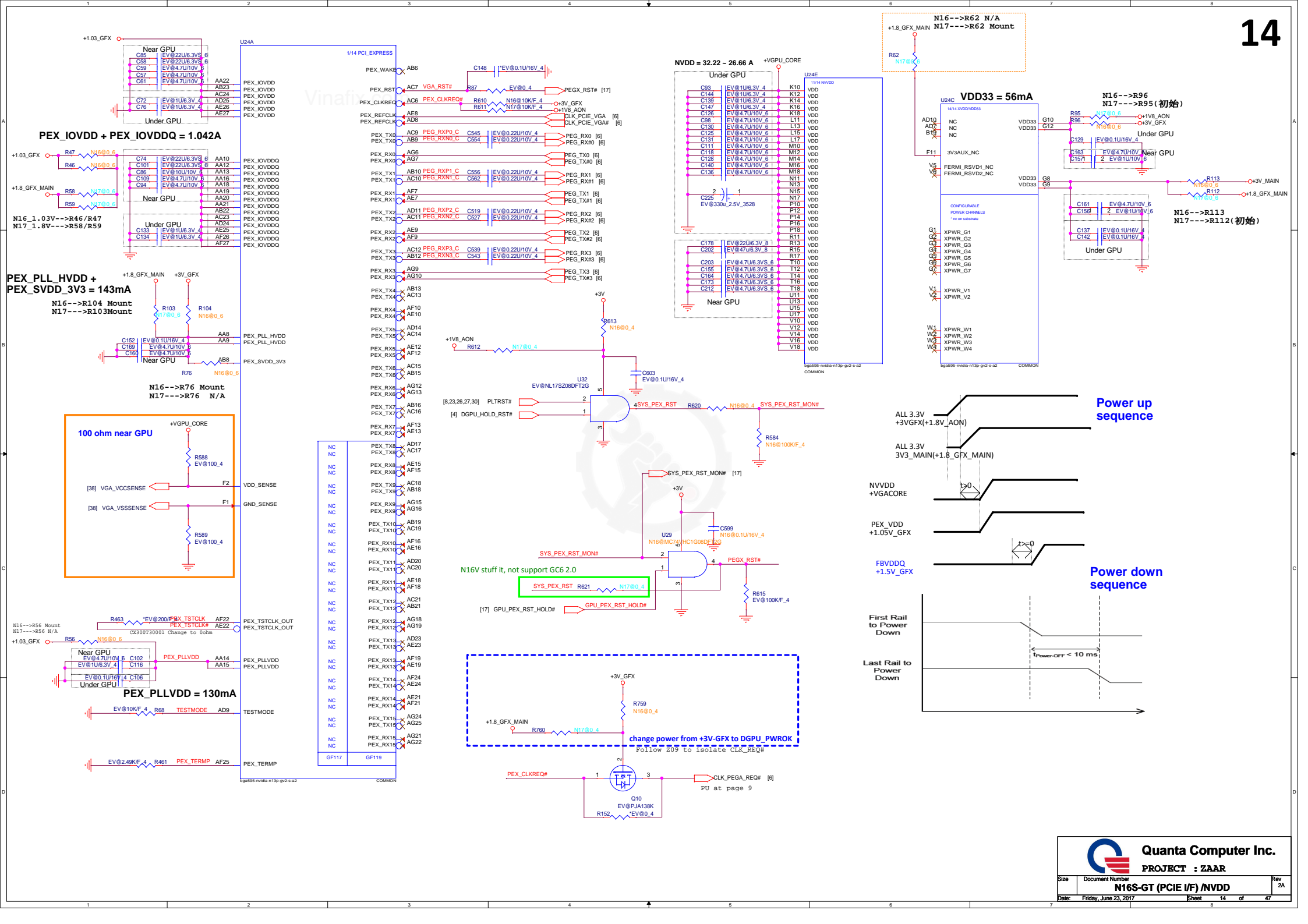


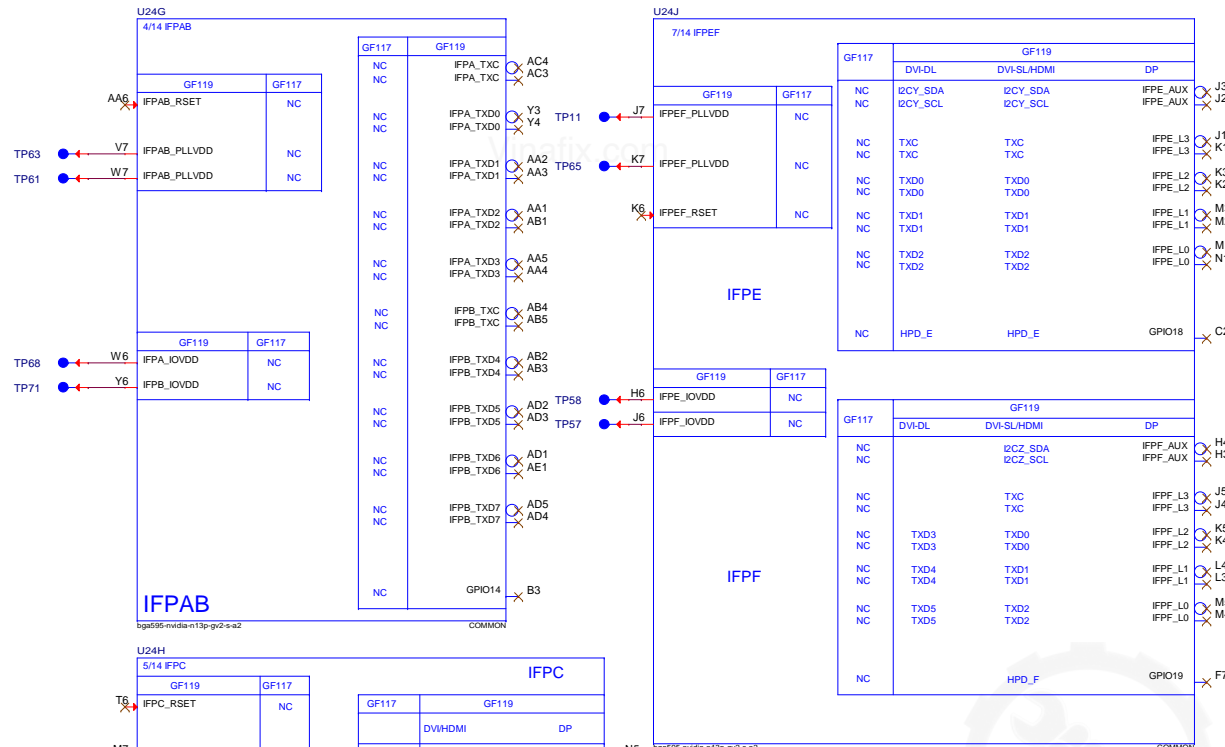
	SA1	SA0
CHA	0	0
CHB	1	0

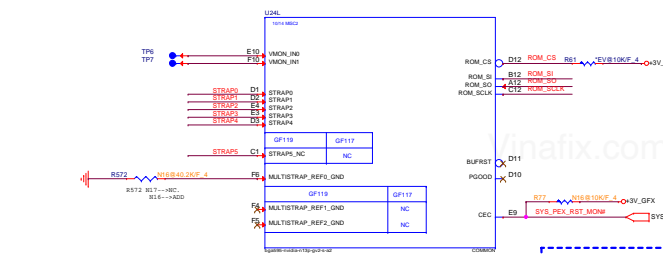


Quanta Computer Inc.

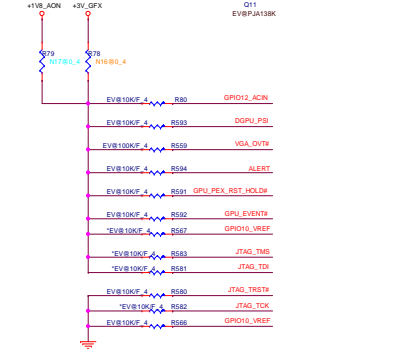
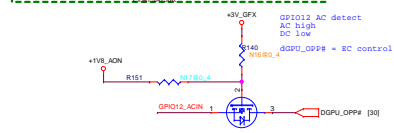
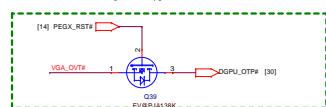
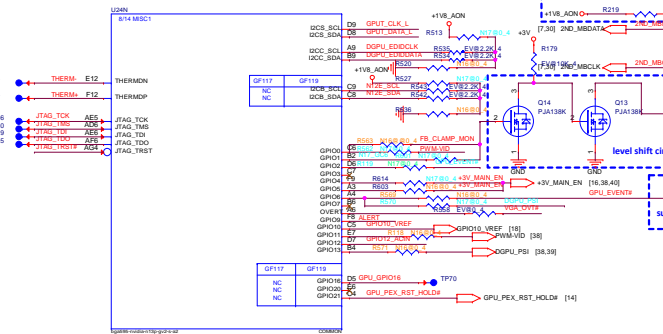
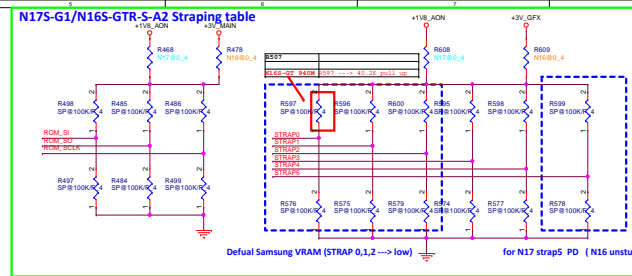
PROJECT : ZRW







N17S-G1/N16S-GT S-A2 Strapping table



GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	OUT	GC6_FB_EN	GC6 FB Enable (GC6 2.0)
5	OUT	+3V_MAIN_EN	Enable GC6 +3V_MAIN
6	IN	DGPU_EVENT#	DGPU EVENT from CPU (GC6 2.0)
8	OUT	VGA_OVTR	ACTIVE LOW THERMAL OVER TEMP
9	OUT	ALERT	ACTIVE LOW THERMAL ALERT
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shading

N16S-GT/N16V-GM Strapping table

ROM_SI N16S-GT [940M]
 2G Hynix 128Mx16 → 34.8K PD
 2G Micron 128Mx16 → 45.3K PD
 2G Samsung 128Mx16 → 4.99K PU
 4G Hynix 256Mx16 → 30.1K PU Single Rank
 4G Hynix 256Mx16 → 24.9K PU Dual Rank
 4G Micron 256Mx16 → 10K PD
 4G Samsung 256Mx16 → 15K PD

ROM_SO
 N16S-GT → 4.99K PD
 N16S-GT → 4.99K PD
 N16S-GT → 40.2K PU

N16S-GT VRAM Configuration Table

ROM_SI

RAMCFG [3:0]	DESCRIPTION	1.35V DDR5	Vendor	Vendor PIN	ROM_SI	STW B/S
0000 0x0	DDR5 256Mx32, 64bit, 8Gb, 2500MHz	SAMSUNG B-die	K4G80325FB-HC03	PD 4.99K ohm	AKG5QGDT502	
0000 0x0	DDR5 256Mx32, 64bit, 8Gb, 3000MHz	SAMSUNG B-die	K4G80325FB-HC28	PD 4.99K ohm	AKG5QGDT518	
0001 0x1	DDR5 256Mx32, 64bit, 8Gb, 2500MHz	Micron A-die	MT51J256M32HF-60A	PD 10K ohm	AKG5LQUTL04	
0001 0x1	DDR5 256Mx32, 64bit, 8Gb, 3000MHz	Micron A-die	MT51J256M32HF-70A	PD 10K ohm	AKG5QGUTL15	
0010 0x5	DDR5 256Mx32, 64bit, 8Gb, 2500MHz	HYNIX M-die	H5GCB824MJR-T2C	PD 30.1K ohm	AKG5QFUTW04	
0010 0x5	DDR5 256Mx32, 64bit, 8Gb, 3000MHz	HYNIX M-die	H5GCB824MJR-R0C	PD 30.1K ohm	AKG5QGUTW06	

N17S-G1-A1 VRAM Configuration Table

STRAP0, STRAP1, STRAP2

RAMCFG [3:0]	DESCRIPTION	1.35V DDR5	Vendor	Vendor PIN	STRAP0	STRAP1	STRAP2	STW B/S
0000 0x0	DDR5 256Mx32, 64bit, 8Gb, 3000MHz	SAMSUNG B-die	K4G80325FB-HC28	PD 100K ohm	PD 100K ohm	PD 100K ohm	PD 100K ohm	AKG5QGDT518
0001 0x1	DDR5 256Mx32, 64bit, 8Gb, 3000MHz	Micron A-die	MT51J256M32HF-70A	PU 100K ohm	PD 100K ohm	PD 100K ohm	PD 100K ohm	AKG5QGUTL15
0010 0x2	DDR5 256Mx32, 64bit, 8Gb, 3000MHz	HYNIX M-die	H5GCB824MJR-R0C	PD 100K ohm	PU 100K ohm	PD 100K ohm	PD 100K ohm	AKG5QGUTW06

N16S-GTR-S-A2 DID=0x1347 [940M]

ROM_SI = VRAM Configuration follow below table
 ROM_SO = Stuff 4.99K pull down
 ROM_SCLK = Stuff 4.99K pull down
 STRAP0 = Stuff 40.2K pull up
 STRAP1 = NC
 STRAP2 = NC
 STRAP3 = NC
 STRAP4 = NC
 STRAP5 = NC

N17S-G1-A1 DID=0x1D10 [1040]

ROM_SI = Stuff 100K pull up
 ROM_SO = Stuff 4.99K pull up
 ROM_SCLK = Stuff 100K pull up and Stuff 100K pull down
 STRAP0 = VRAM Configuration follow below table
 STRAP1 = VRAM Configuration follow below table
 STRAP2 = VRAM Configuration follow below table
 STRAP3 = Stuff 100K pull down
 STRAP4 = Stuff 100K pull down
 STRAP5 = Stuff 100K pull down

Note: GC6 2.0 is supported by N16x GPU in the GB28, GB48-128, and GB38-256 packages.

Logical Strap Bit Mapping

Resistor P/N	PU-VDD	PD
4.99K → CS24992FB26	1000	0000
10K → CS31002FB26	10K	0001
15K → CS31502FB24	15K	0010
20K → CS32002FB29	20K	0011
24.9K → CS32492FB16	24.9K	0100
30.1K → CS33012FB18	30.1K	0101
34.8K → CS33482FB22	34.8K	0110
40.2K → CS34022FB15	40.2K	0111
45.3K → CS34532FB15	45.3K	1100
49.9K → CS34992FB10	49.9K	1111

N16S-GTR-S-A2 PN: AJ0N16S0T44

N17S-G1-A1 PN: AJ0N17S0T01

Non-mirror, MF=0
Channel A
<0-31>

Mirror, MF=1
Channel A
<32-63>

Channel A
<32-63>

DQA24~31

DQA16~23

DQA8~15

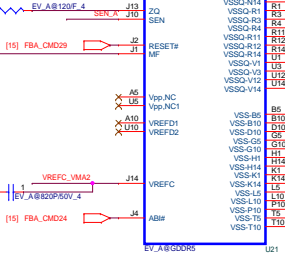
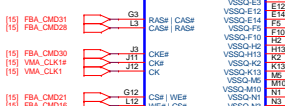
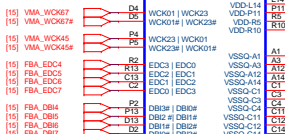
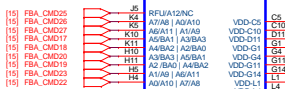
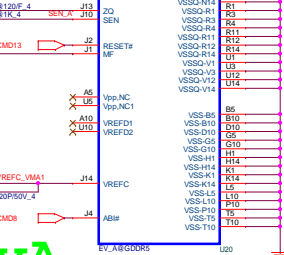
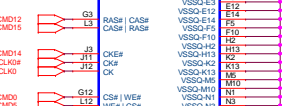
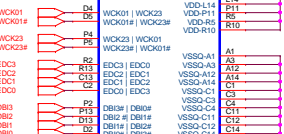
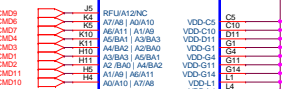
DQA0~7

DQA32~39

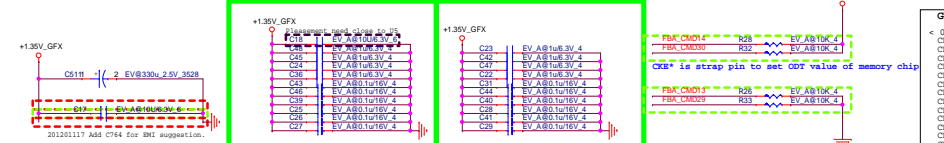
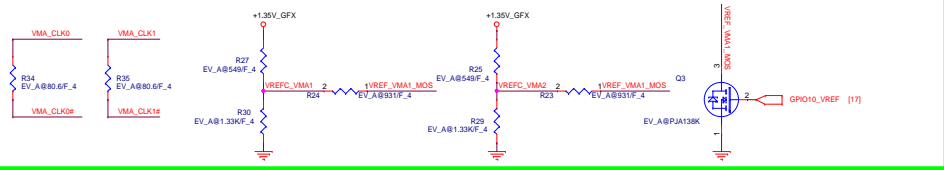
DQA40~47

DQA48~55

DQA56~63



KB OnlyA



GDDR5 Mode H Mapping

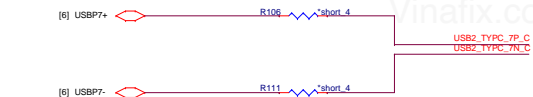
Channel	Bank	Memory
< 0-31 >	< 32-63 >	Memory
CHD0	CHD16	CS*
CHD1	CHD17	A3_BA3
CHD2	CHD18	A2_BA0
CHD3	CHD19	A4_BA2
CHD4	CHD20	A5_BA1
CHD5	CHD21	WE*
CHD6	CHD22	A7_A8
CHD7	CHD23	A6_A11
CHD8	CHD24	AB*
CHD9	CHD25	A12_RPT
CHD10	CHD26	A0_A10
CHD11	CHD27	A1_A9
CHD12	CHD28	RA*
CHD13	CHD29	RST*
CHD14	CHD30	CKE*
CHD15	CHD31	CA*

RST PD place @ the end of daisy-chain.

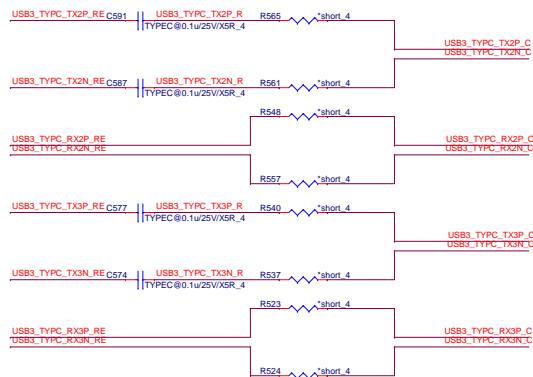
USB TYPE-C

USB2.0 ESD

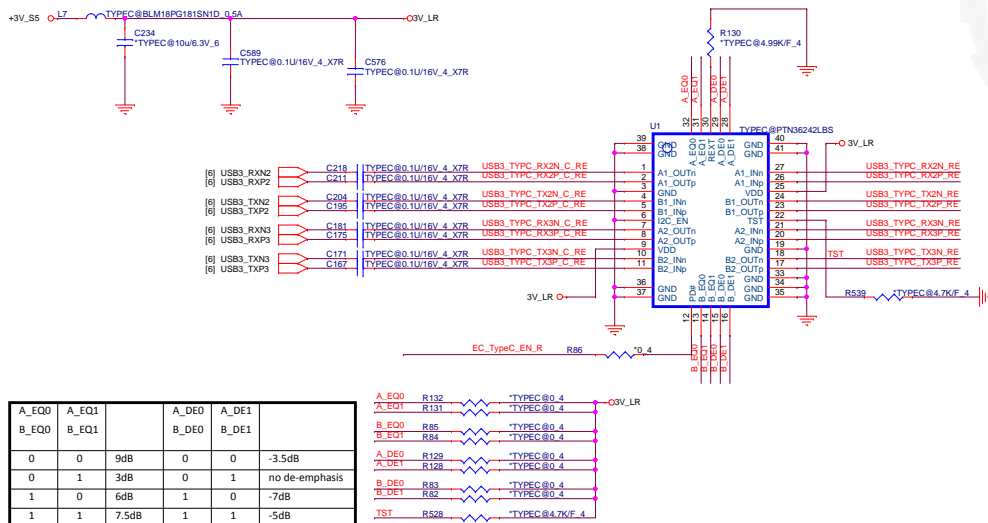
Close to connector



Type C1 HSIO ESD



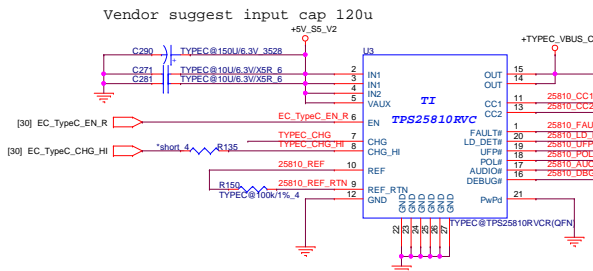
USB3 Re-Driver



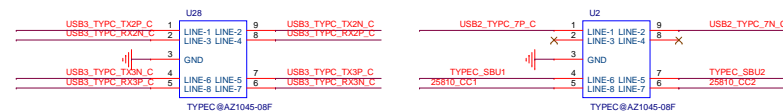
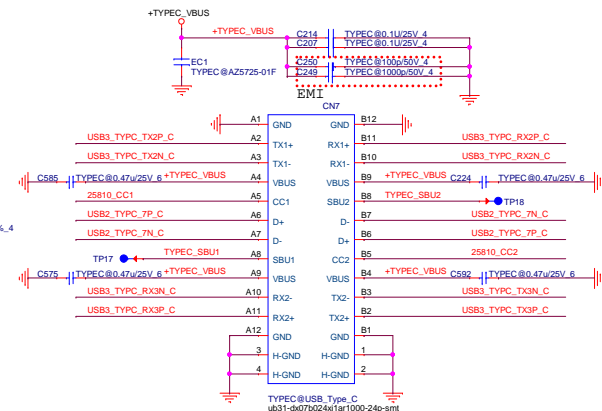
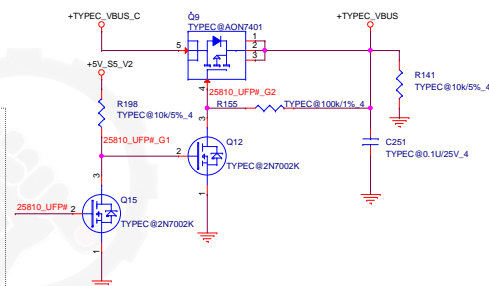
A_EQ0 B_EQ0	A_EQ1 B_EQ1		A_DE0 B_DE0	A_DE1 B_DE1	
0	0	9dB	0	0	-3.5dB
0	1	3dB	0	1	no de-emphasis
1	0	6dB	1	0	-7dB
1	1	7.5dB	1	1	-5dB

TST : Low = Normal LFPS swing / Hight = Turn down LFPS swing

[2,3,4,6,7,8,9,11,23,26,27,28,30,31,33,39] +3V_S5
[31] +5V_S5 V2



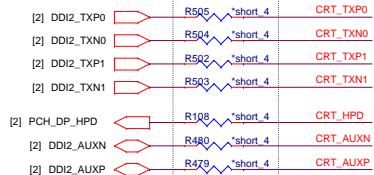
TPS25810 Port	CC1	CC2	OUT	TPS25810 Response				
				VCONN on CC1 or CC2	POLs	UFPs	AUDIOS	DEBUR
Nothing Attached	OPEN	OPEN	OPEN	NO	H-Z	H-Z	H-Z	H-Z
UFP Connected	Rd	OPEN	IN1	NO	H-Z	LOW	H-Z	H-Z
UFP Connected	OPEN	Rd	IN1	NO	LOW	LOW	H-Z	H-Z
Powered Cable No UFP Connected	OPEN	Rd	IN1	NO	LOW	H-Z	H-Z	H-Z
Powered Cable No UFP Connected	Ra	OPEN	OPEN	NO	H-Z	H-Z	H-Z	H-Z
Powered Cable UFP Connected	Rd	OPEN	IN1	NO	H-Z	LOW	H-Z	H-Z
Powered Cable UFP Connected	Ra	OPEN	IN1	NO	H-Z	LOW	H-Z	H-Z
Powered Cable UFP Connected	Rd	IN1	CC1	LOW	H-Z	H-Z	H-Z	H-Z
Debus Accessory Connected	Rd	Rd	OPEN	NO	H-Z	H-Z	LOW	LOW
Debus Accessory Connected	Ra	Rd	OPEN	NO	H-Z	H-Z	LOW	LOW



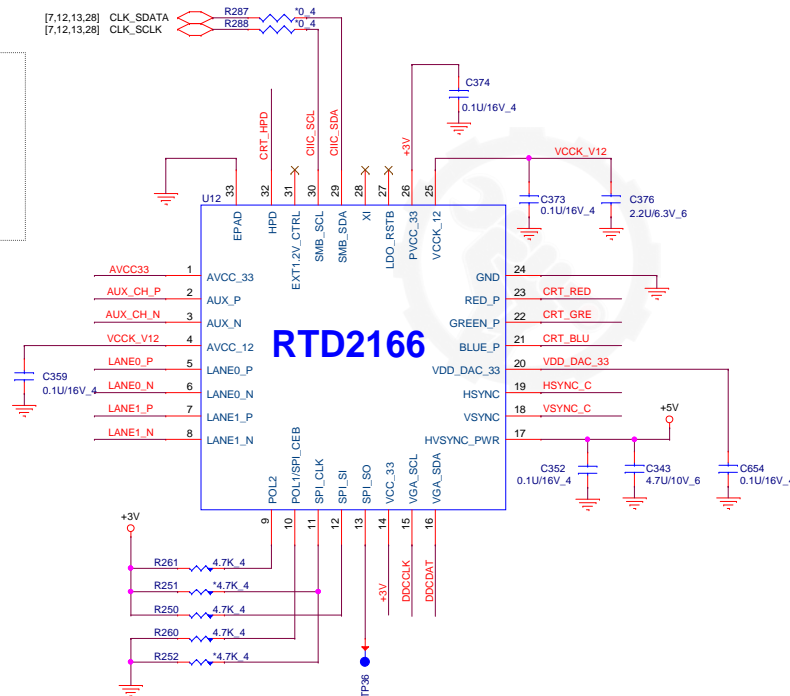
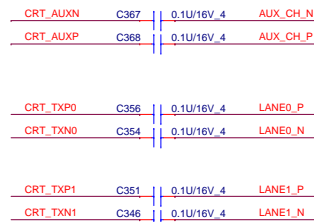
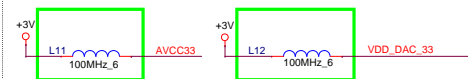
Quanta P/NAMAZING P/NUSD保護位置
BC104308Z00AZ1043-08F.R7G0.08TX RX (USB3.0 GEN1 5G)
BC104508Z00AZ1045-08F.R7G0.08D+ D- SBU1 SBU2 CC1 CC2
BC005725Z00AZ5725-01F.R7G0.009 PD 5V (follow ZAA)

DP TO VGA

Close to CPU side of CAP.



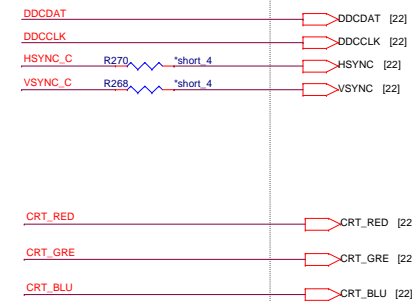
Power



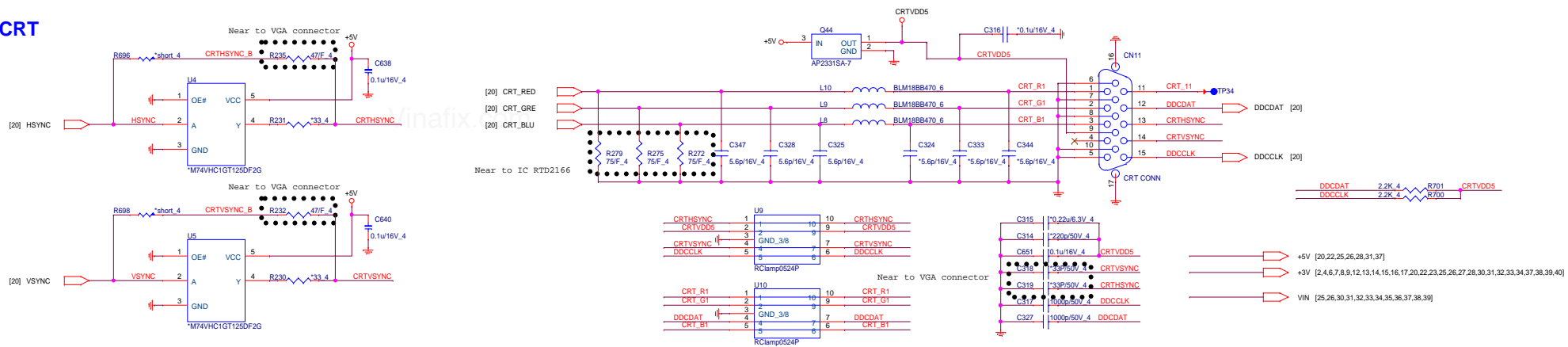
Note:

- 1- C1,C3,C4,C5,C11,C16, C21 should be placed close to chip
- 2- C5 should be X5R material
- 3- R6, R7, R8 should be 75 ohm with +/-1%
- 4- Suggest to connect Pin 29 and Pin 30 to PCH SMBUS for debug purpose.
- 5- This configuration is for internal ROM mode and using embedded LDO mode.

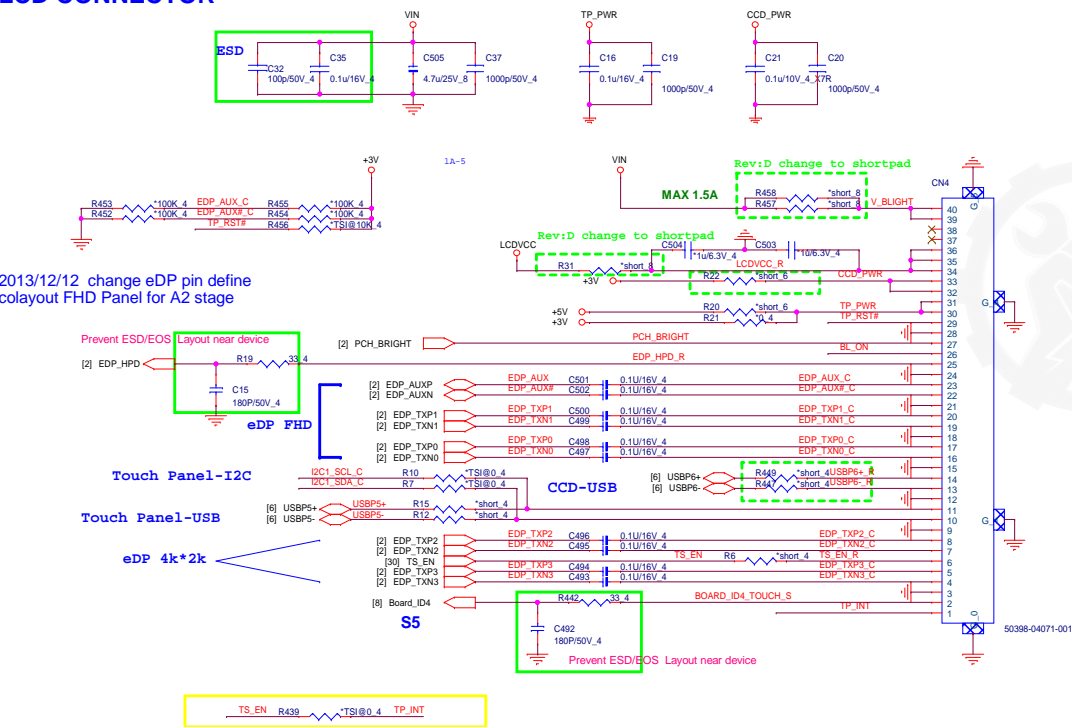
VGA



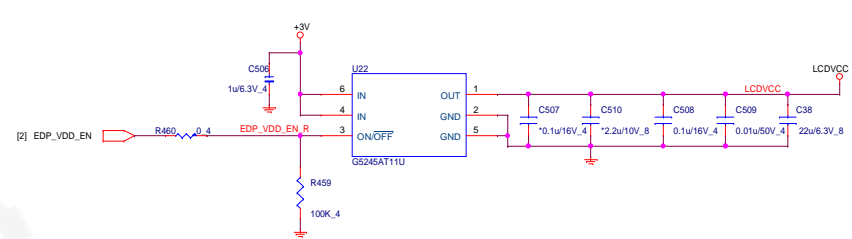
CRT



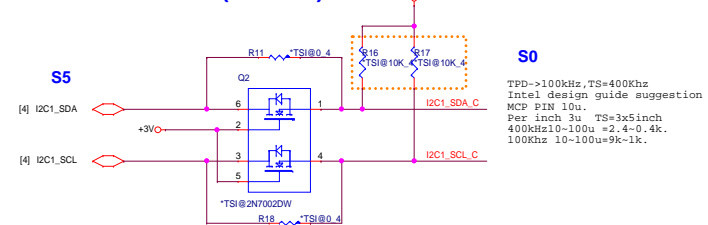
LCD CONNECTOR



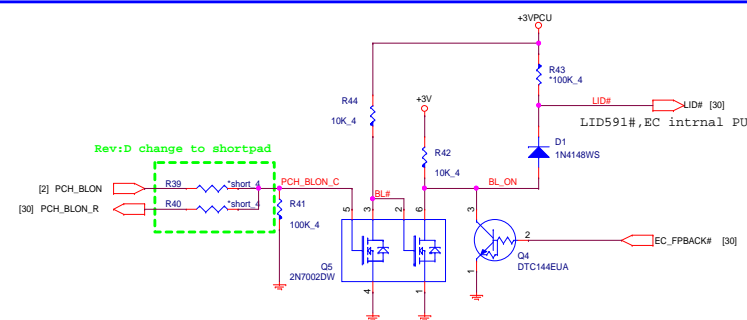
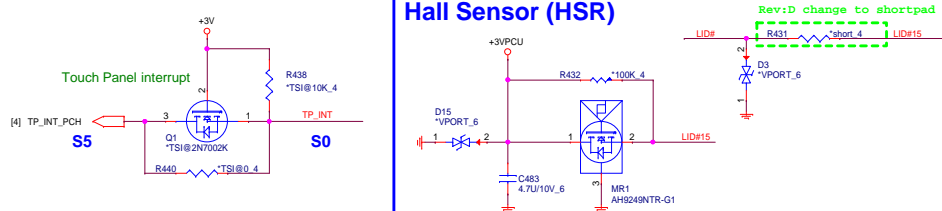
LCD Power



Touch screen level shift I2C(reserve)

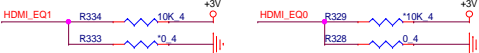


Hall Sensor (HSR)



HDMI

OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode; DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode

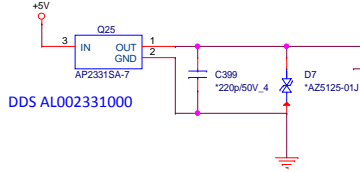
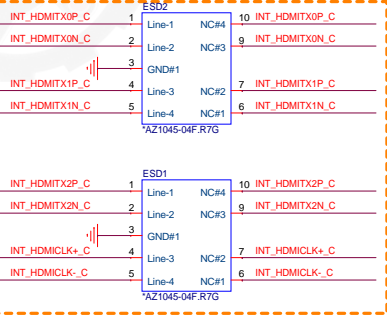
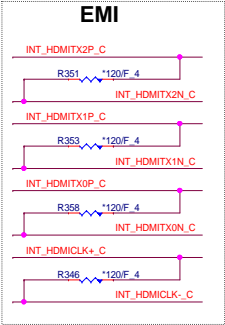
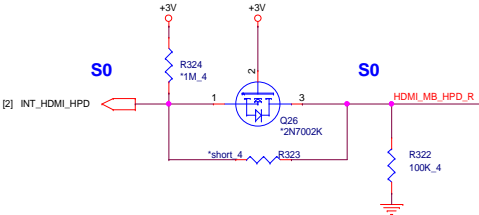
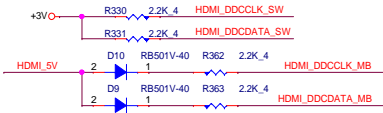
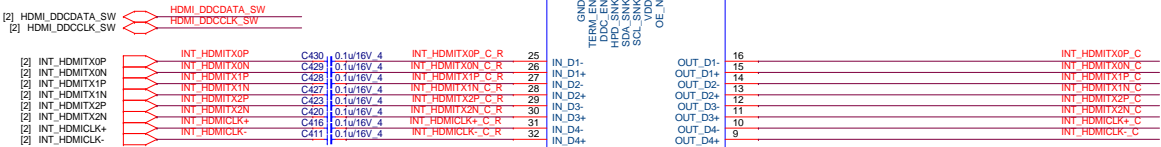


The PTN3366 supports four level equalization settings based on binary input pins EQ0 and EQ1.

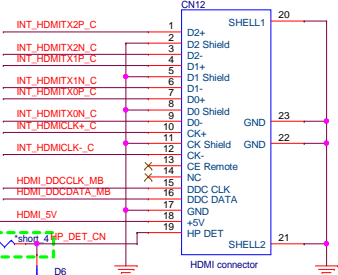
Table 5. Equalizer settings

Inputs		Equalization for 3 Gbit/s
EQ1	EQ0	
short to GND	short to GND	0 dB
short to GND	short to VDD	2 dB
short to VDD	short to GND	4 dB
short to VDD	short to VDD	6 dB

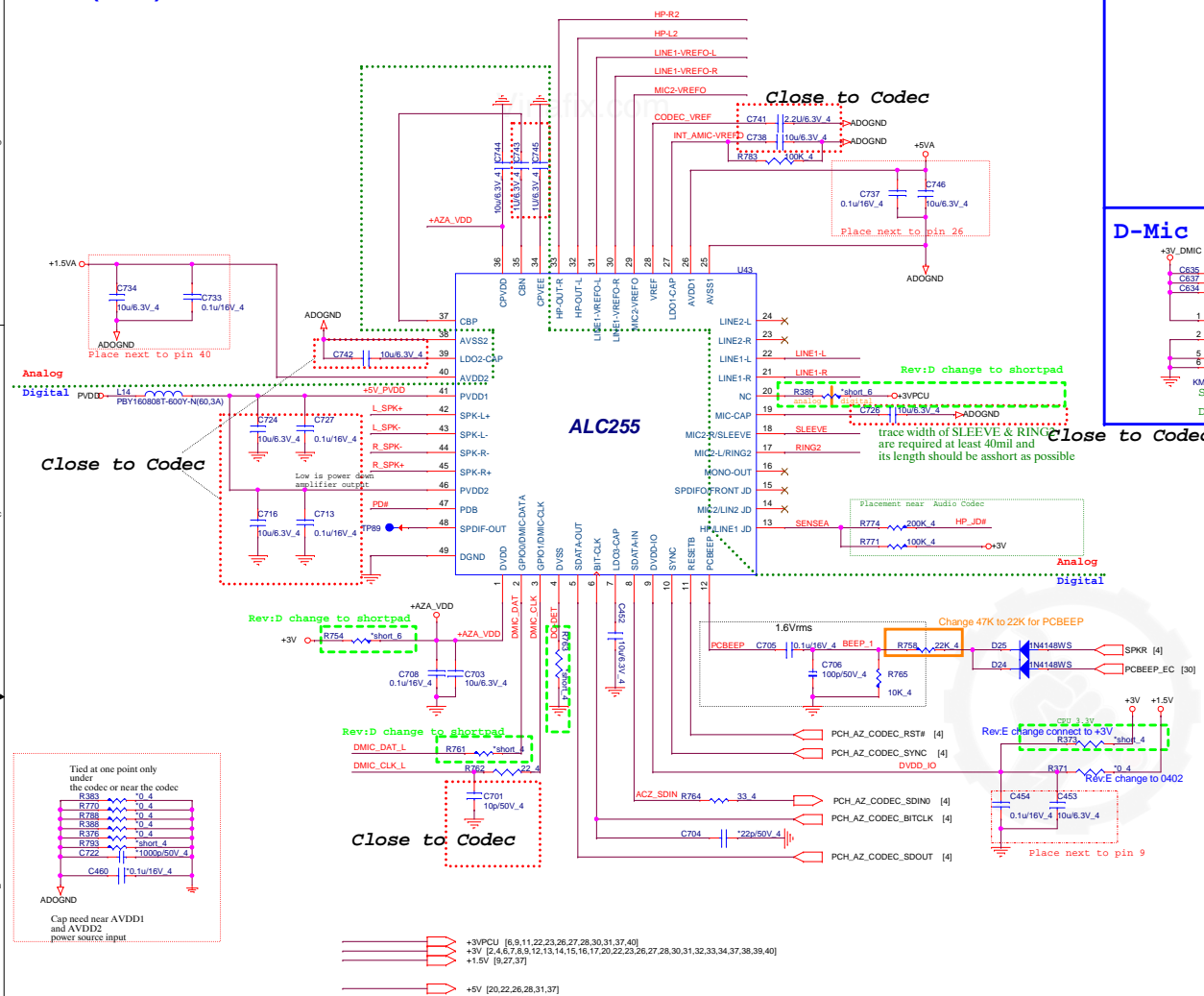
From PCH



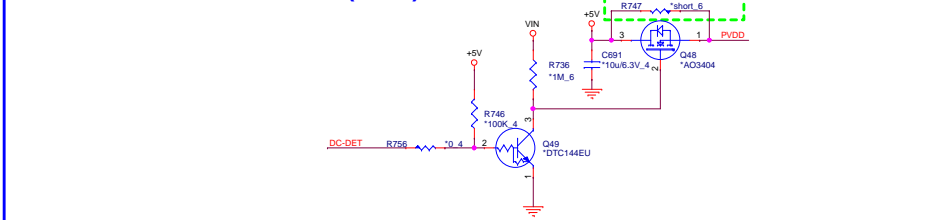
HDMI connector



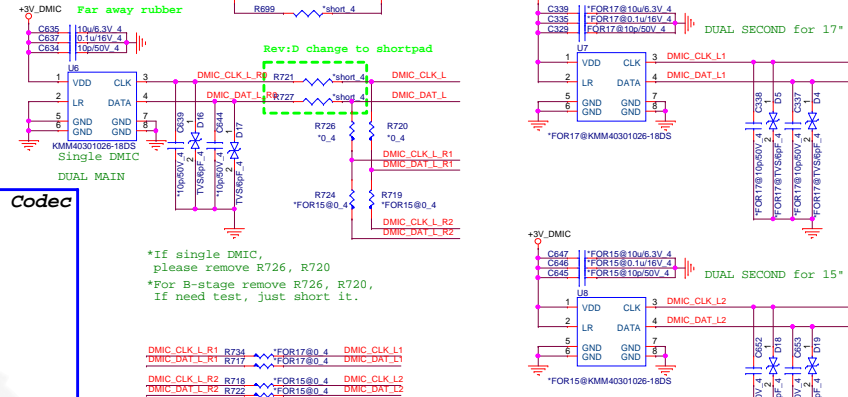
Codec(ADO)



DC-DET circuit(ADO)



D-Mic (MIC)

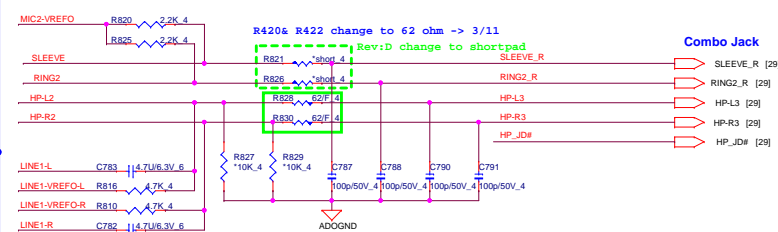


Single DMIC and Dual DIMC same PN: AL403010A00

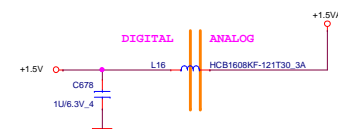
- ```
1.Single DMIC
NSM0407DT (AL472376000) <- Main source
SPM0437HD4H (AL000437000)

2.Dual DMIC
NSM0410DT (W/ Fortemedia algorithm)
Main MIC SC need connect to second MIC DATA
```

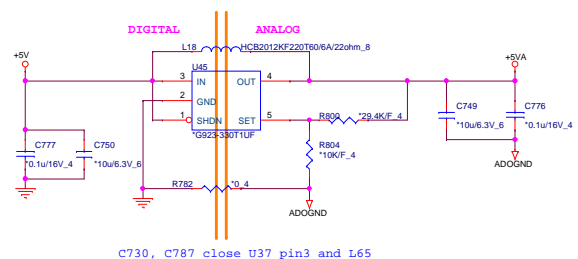
### Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)



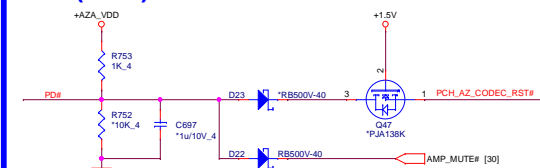
### Codec PWR 1.5V(ADO)



### Codec PWR 5V(ADO)

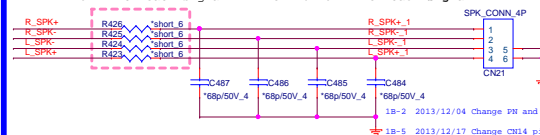


## Mute(ADO)



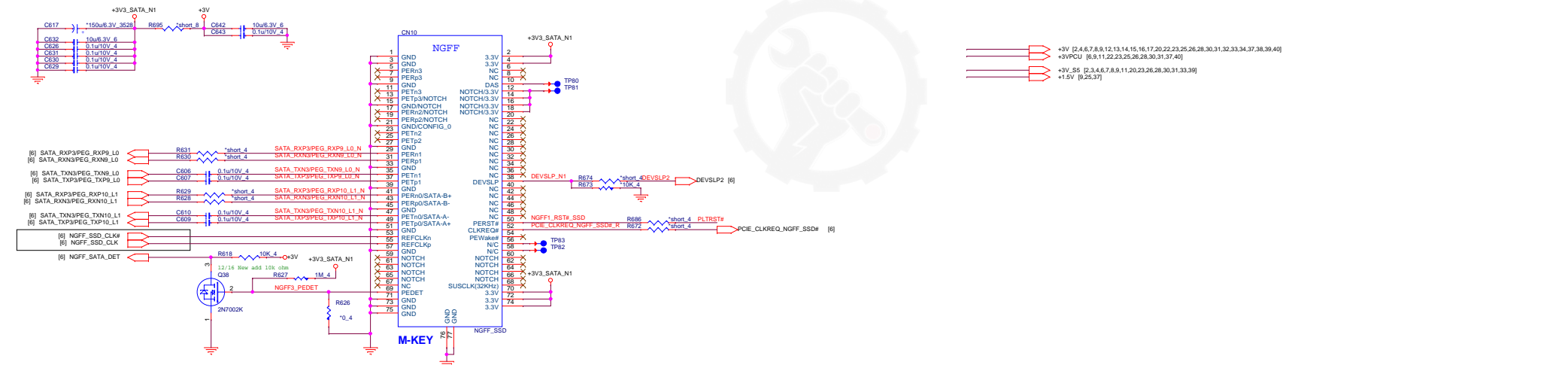
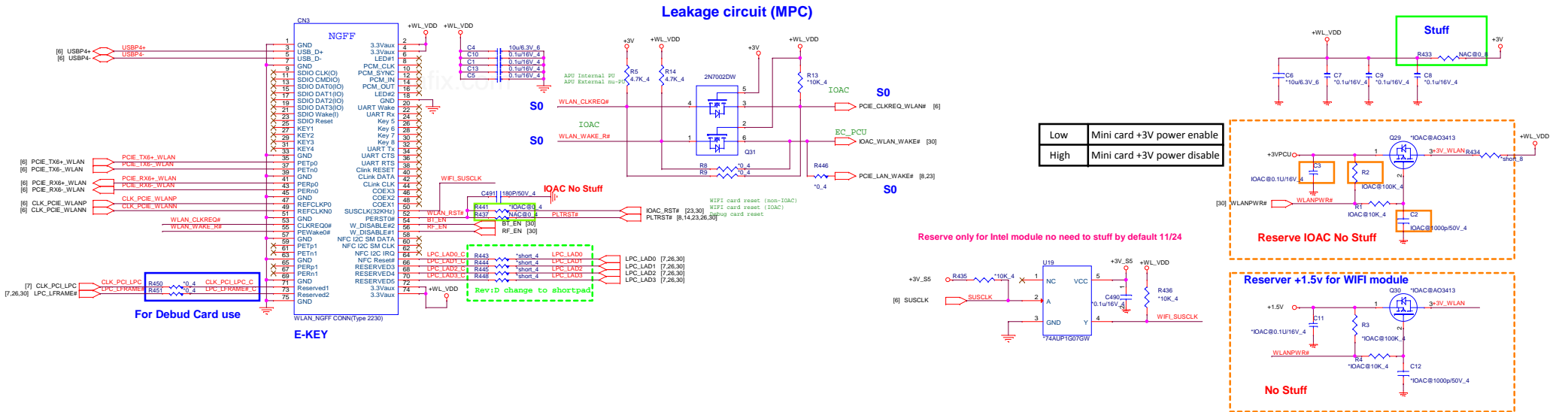
## Internal Speaker

40mil for each signal      4 ohm : 40mil for each signal

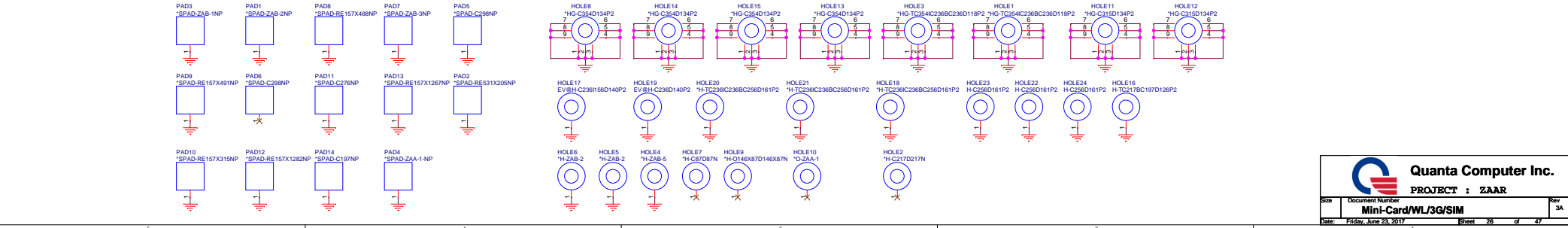




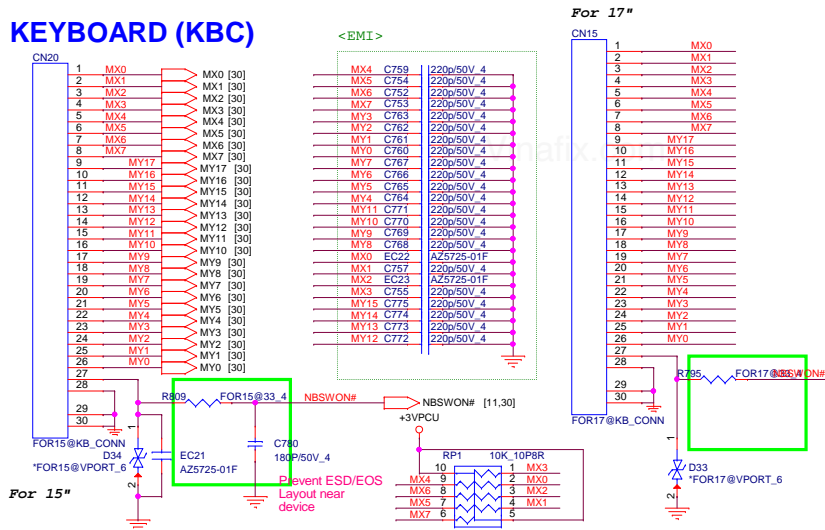
## NGFF\_M.2 WiFi & BT (NGF)



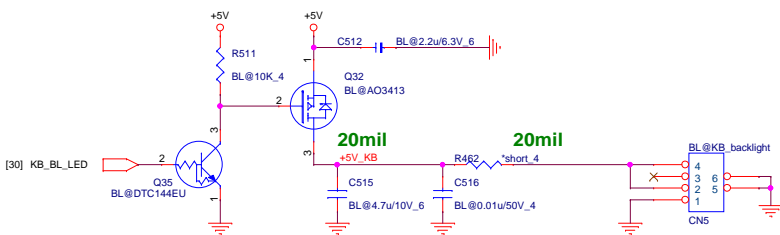
## PAD and HOLE



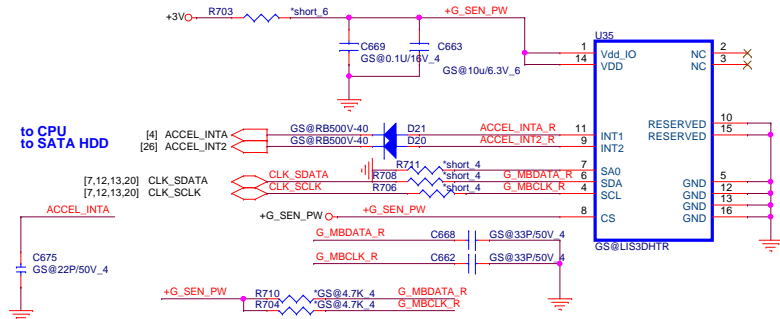
## KEYBOARD (KBC)



**KB\_BL LED (KBC)**

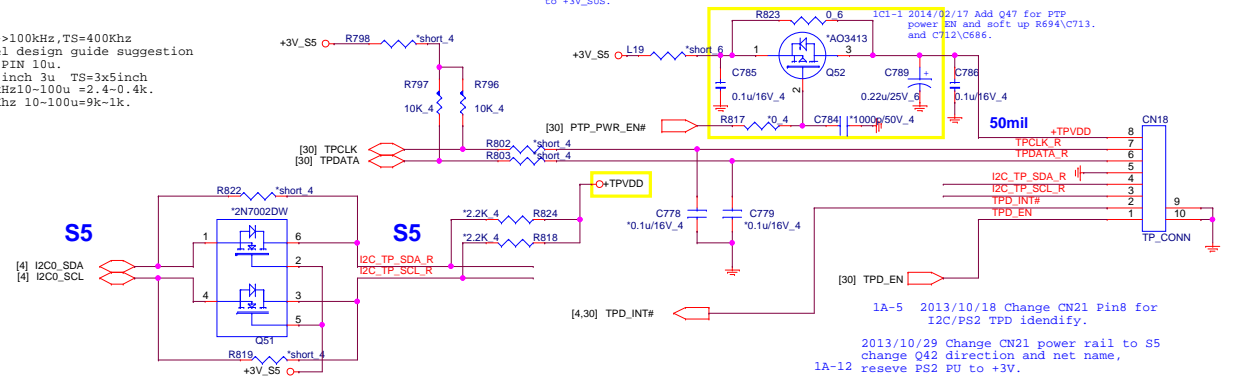


## G-sensor(ACS)



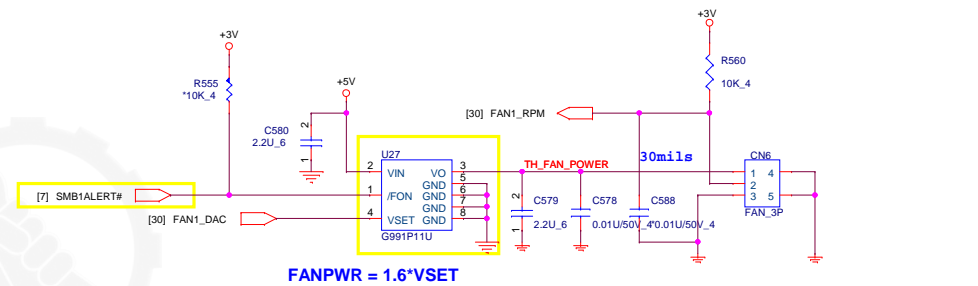
### TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)

TPD->100kHz, TS=400Khz  
Intel design guide suggestion  
MCP PIN 10u.  
Per inch 3u TS=3x5inch  
400kHz10-100u =2.4-0.4k.  
100kHz 10-100u=9k~1k.



## CPU FAN (THM)

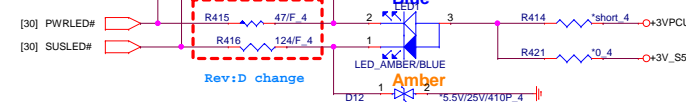
Prevent ESD/EOS  
Layout near  
device



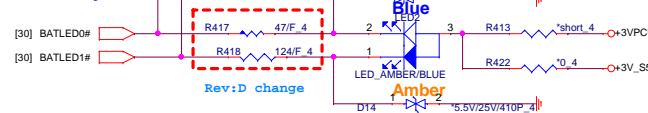
## POWER LED(UIF)

Blue 47 ohm CS04702FB16 -> 2/16 Rev D.

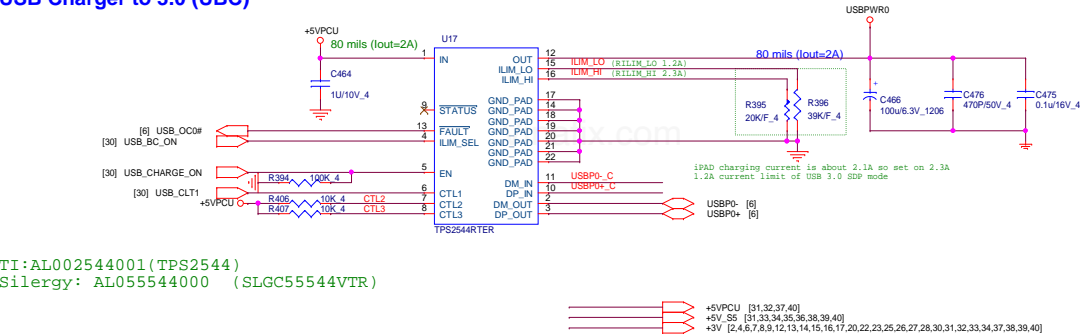
Amber 124 ohm CS11242FB10 -> 2/16 Rev D



## Battery



USB Charger to 3.0 (UBC)



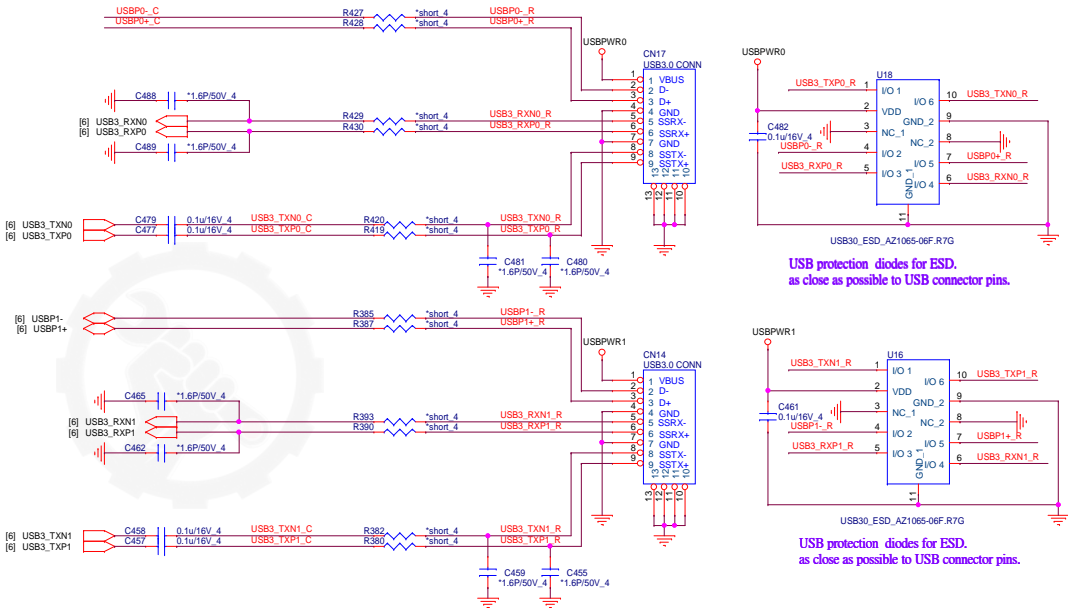
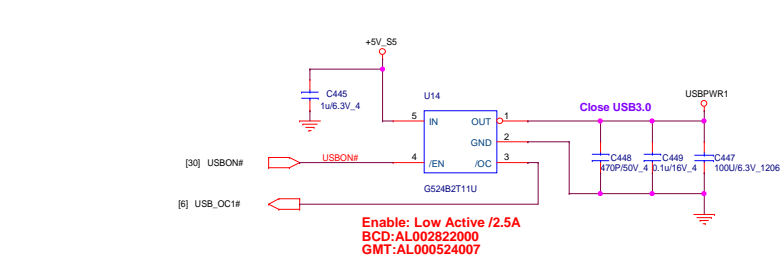
|     | CTL1 | CTL2 | CTL3 | ILIM_SEL |
|-----|------|------|------|----------|
| SDP | 1    | 1    | 1    | 0        |
| CDP | 1    | 1    | 1    | 1        |
| DCP | 0    | 1    | 1    | X        |

RILIM\_LO is optional and the ILIM\_LO pin may be left unconnected if the following conditions are met:

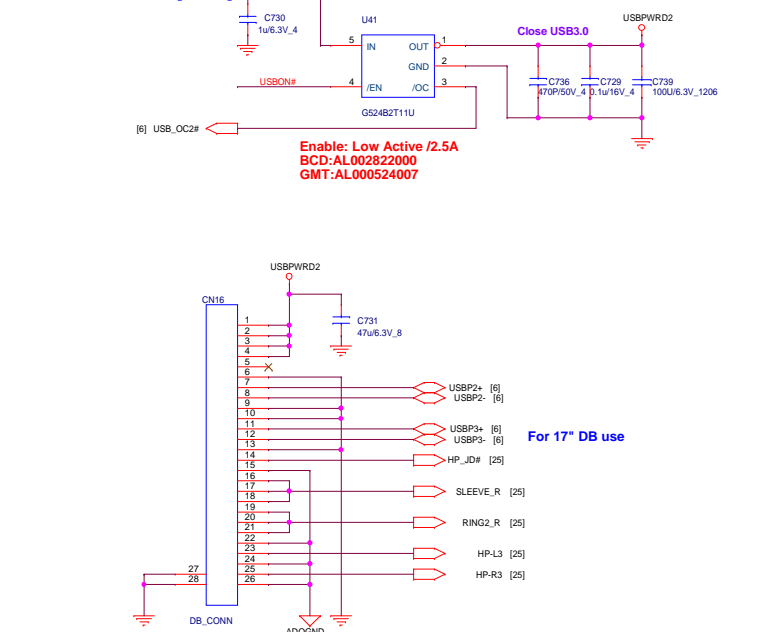
1. ILIM\_SEL is always set high
  2. Load Detection - Port Power Management is not used
  3. Mouse / Keyboard wake function is not used
- If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM\_LO < 80.6 kΩ.
- The following equation programs the typical current limit:
- (1)  $IOS\_typ(mA) = 50,250 / (RILIM\_XX(K\Omega) + 0.1)$
- RILIM\_XX corresponds to either RILIM\_HI or RILIM\_LO as appropriate.

$IOS\_typ(mA) = 50,250 / (RILIM\_XX(K\Omega) + 0.1)$

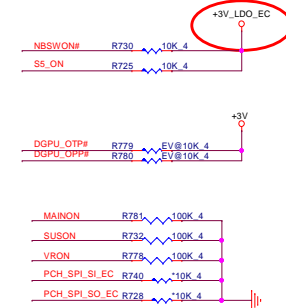
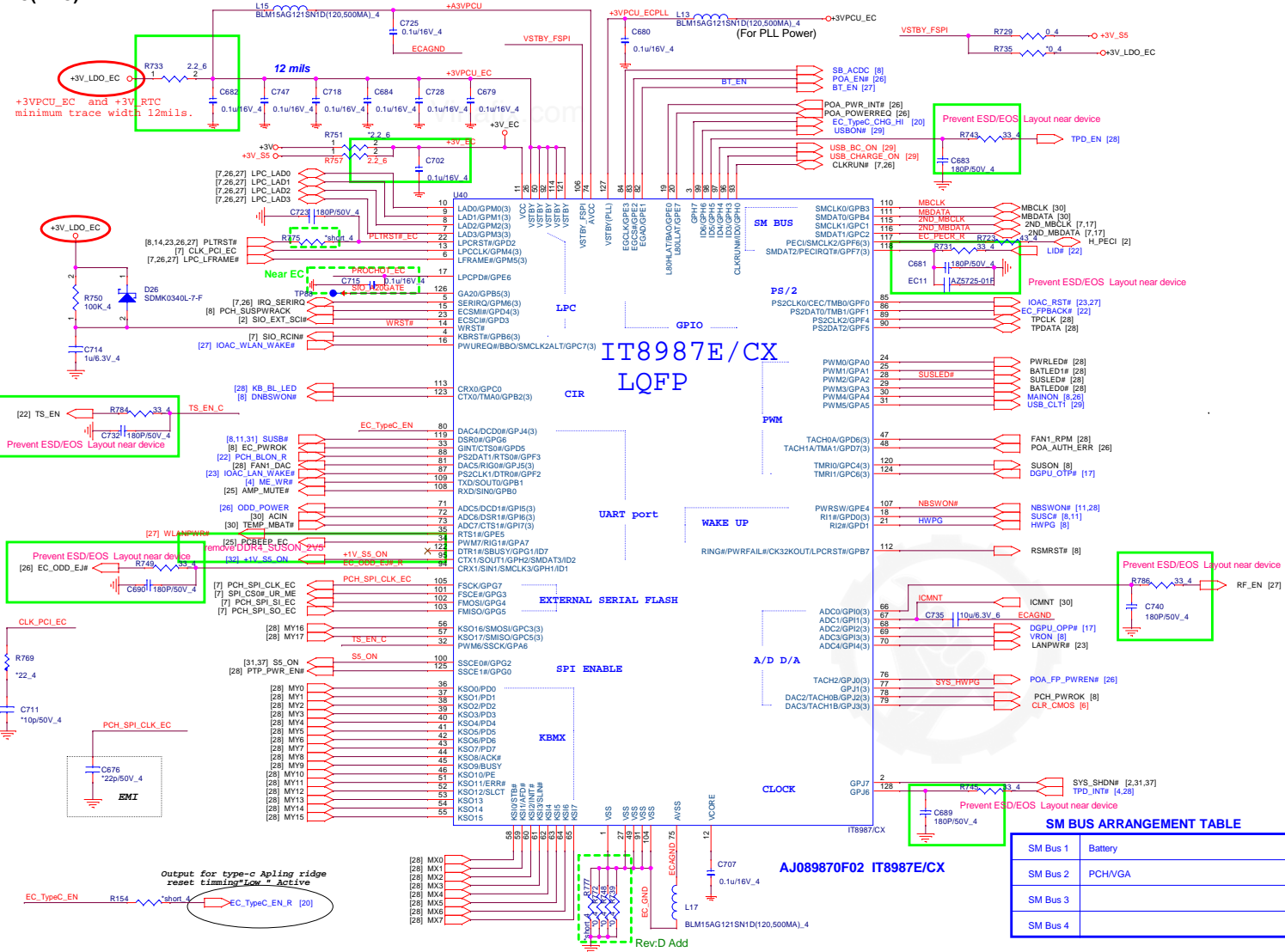
USB 3.0 Connector (UB3)



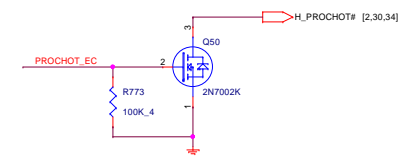
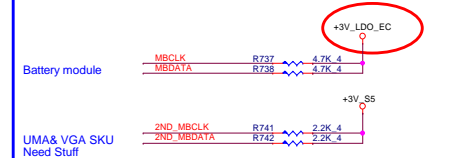
USB2.0 DB (UB2)





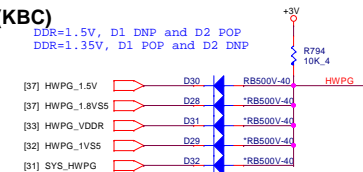


## SM BUS PU(KBC)



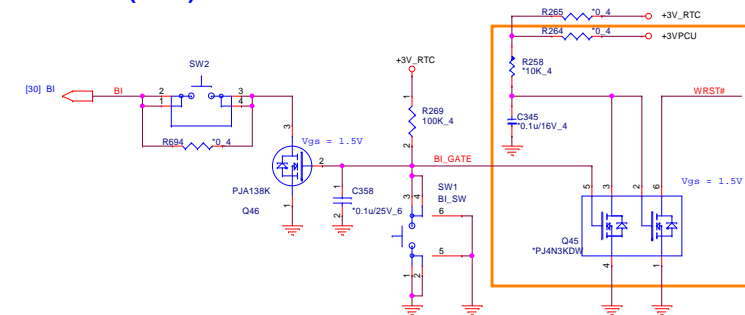
## HWPG(KBC)

DDR=1.5V, D1 DNP and D2 POP  
DDR=1.35V, D1 POP and D2 DNP

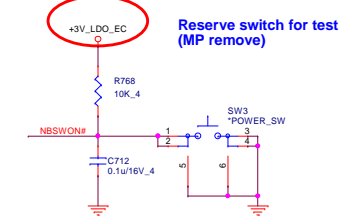
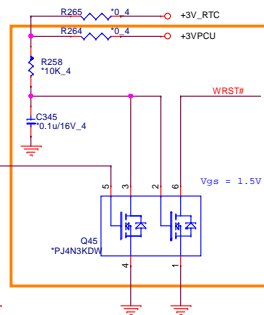


|          |         |
|----------|---------|
| SM Bus 1 | Battery |
| SM Bus 2 | PCH/VGA |
| SM Bus 3 |         |
| SM Bus 4 |         |

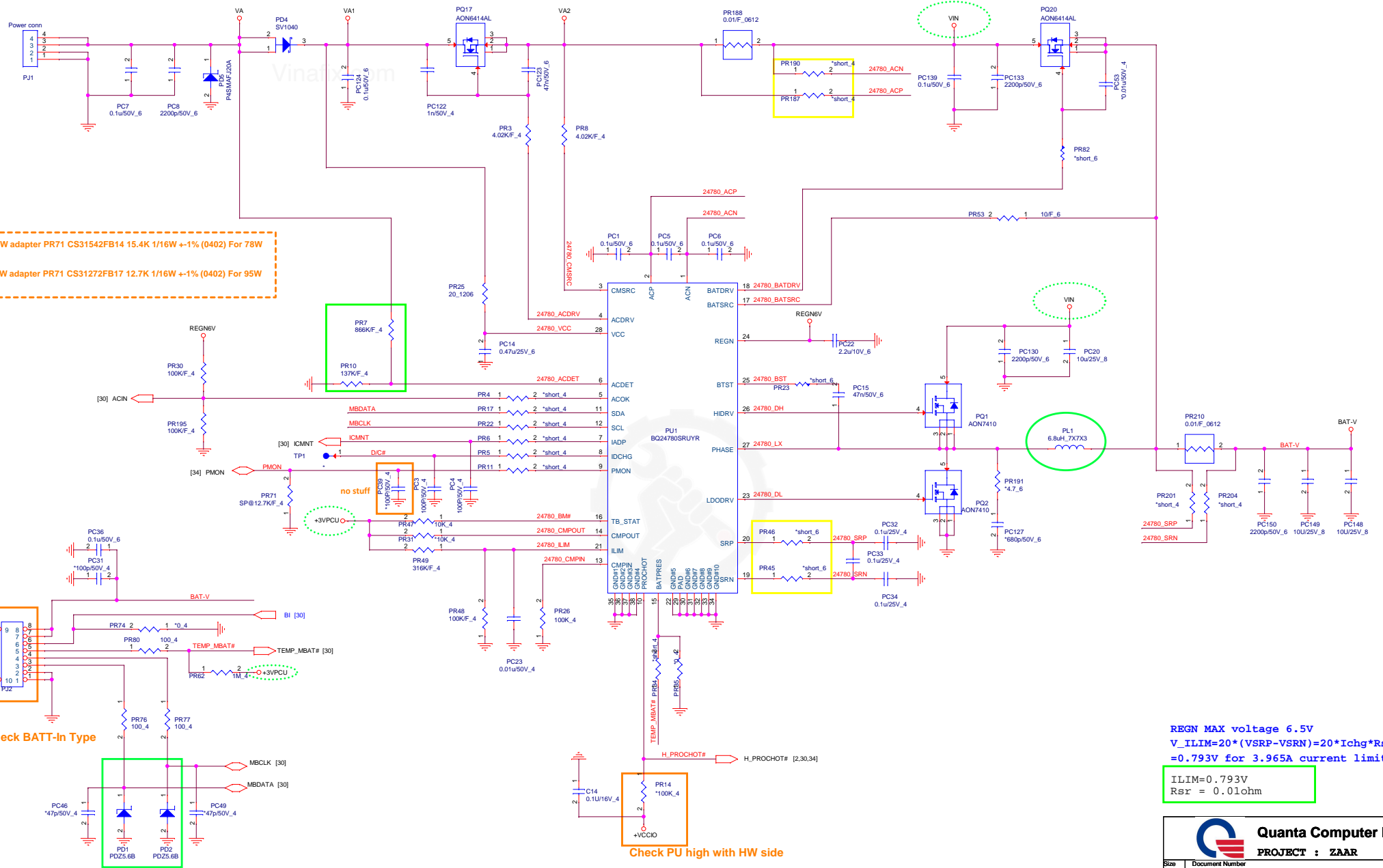
## Reset SW (FSW)



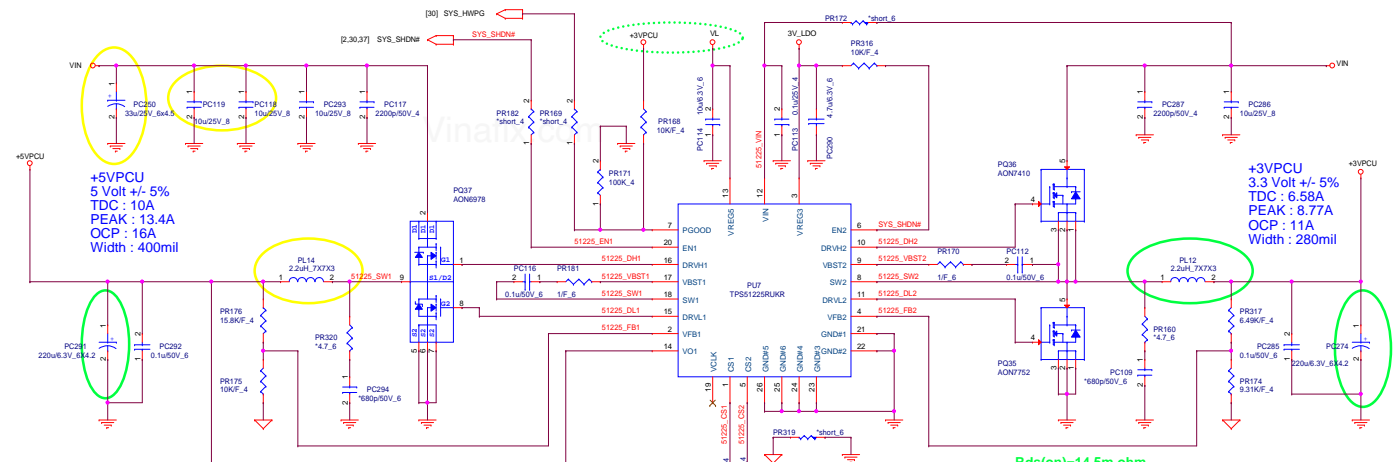
## Battery Detect Switch



# Double Check ADP-In Type



REGN MAX voltage 6.5V  
 $V_{ILIM} = 20 \cdot (V_{SRP} - V_{SRN}) = 20 \cdot I_{chg} \cdot R_{sr}$   
 $I_{LIM} = 0.793V$  for 3.965A current limit  
 $R_{sr} = 0.01ohm$



**OCP:16A**  
L(ripple current)  
= $(9.5)^2/5/(1u0.3M^9)$   
=7.407A  
Iocp= $18-(7.407/2)=12.296A$   
Vth= $(12.296A*4.9mOhm)+1mV=61.252mV$   
R(IIim)=( $61.252mV^8/10uA$   
=49K

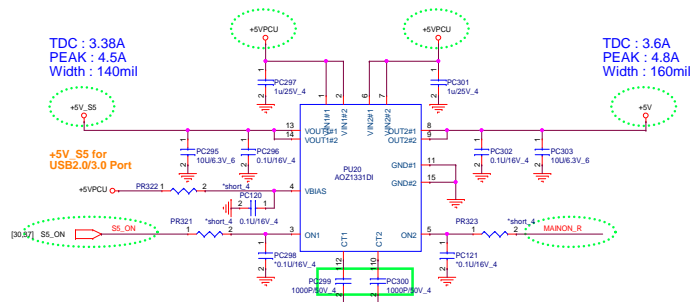
Rds(on)=4.9m ohm

Power auto recovery

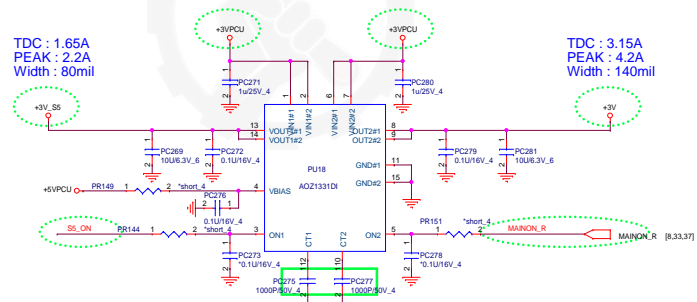


**OCP:11A**  
L(ripple current)  
= $(9.3.3)^2/3.3/(2.2u0.355M^9)$   
=2.676A  
Iocp= $11-(2.676/2)=9.662A$   
Vth= $(9.662A*14.5mOhm)+1mV=141.099mV$   
R(IIim)=( $141.099mV^8/10uA$   
=112.88K

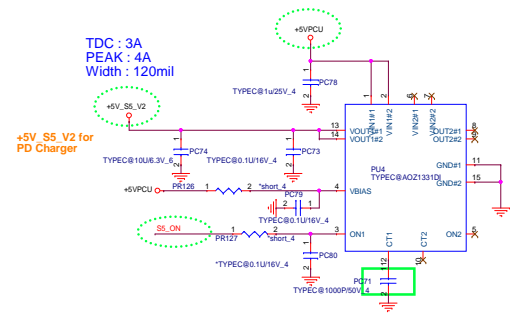
Rds(on)=14.5m ohm



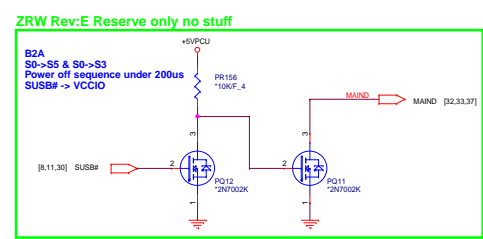
Soft-Start

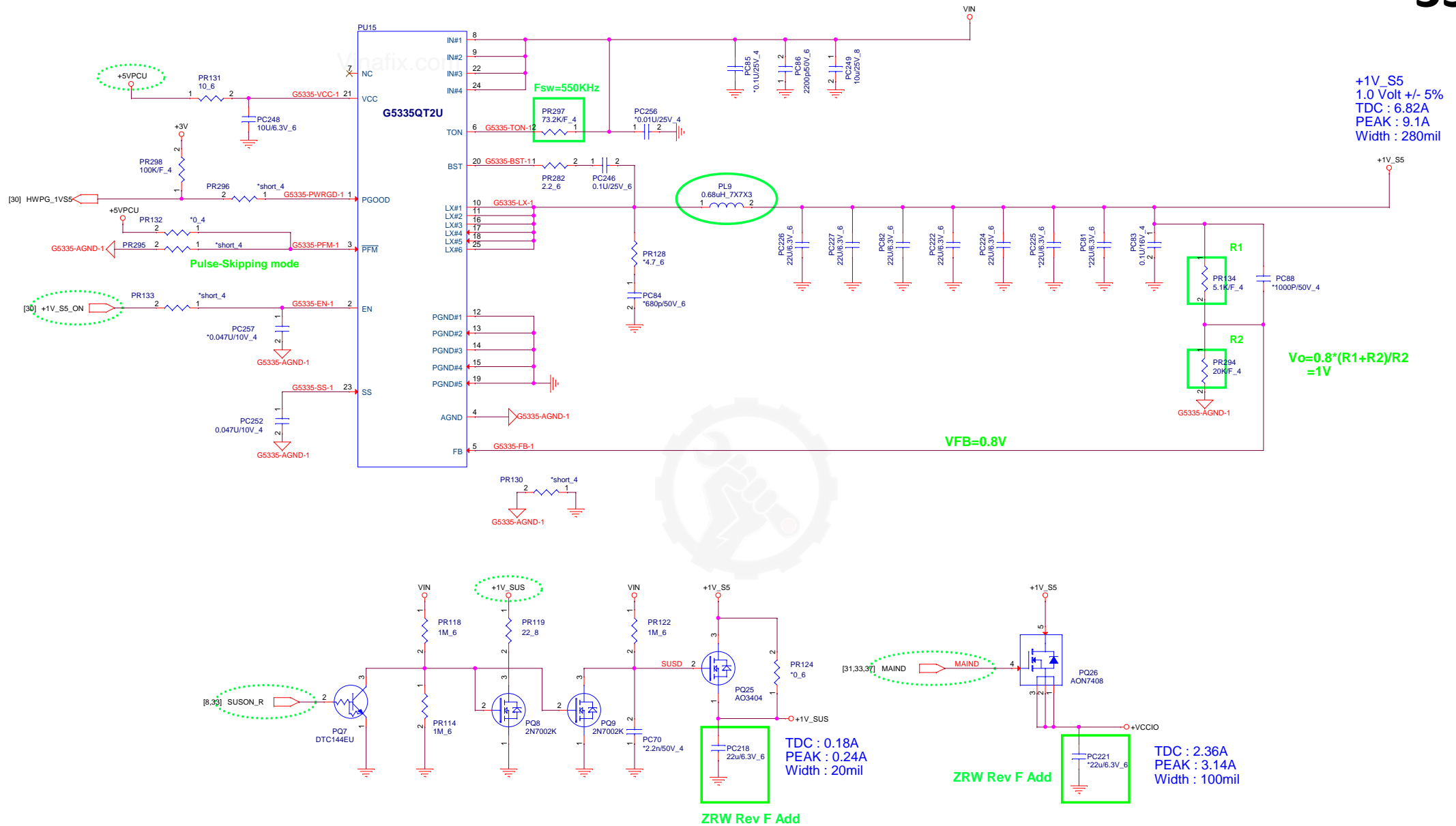


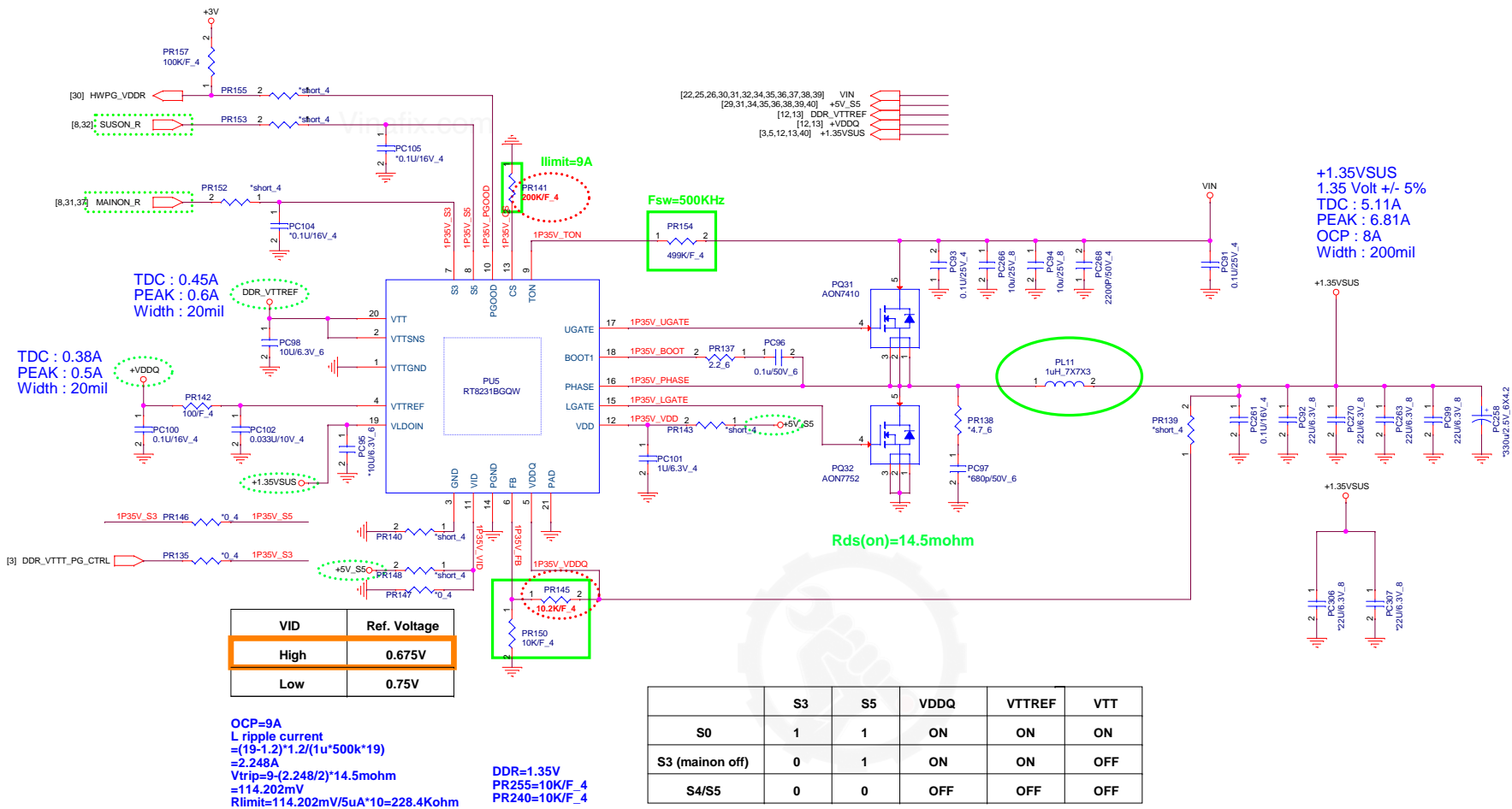
Soft-Start



Soft-Start







remove +2.5VSUS Power circuit 5/2

Check PU high with HW

ZAAA 6L power solution table

## IMVP8 Vcore Controller

Rail A (1 phase) : VCCGT  
Rail B (2 phase) : VCORE  
Rail C (1 phase) : VCCSA

|                                                                                                                                                                    |                                                                                                                                                                                  |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| U22 : PC147 CH4104K9B03 0.1uF/25V<br>U22 : PR79 CS00002JB38 0 ohm<br>U22 : PR224 CS21542FB00 1.54K<br>U22 : PR221 CS12872FB18 287<br>U22 : PR208 CS38872FB18 88.7K | U42 : PC147 CH4152K9B02 0.15uF/10V<br>U42 : PR79 Unstuf<br>U42 : PR224 CS23092FB00 3.09K<br>U42 : PR221 CS13572FB10 357<br>U42 : PR208 CS39312FB15 93.1K                         |
| U22 : PR231 Unstuf<br>U22 : PC45 Unstuf<br>U22 : PC40 Unstuf<br>U22 : PC38 Unstuf<br>U22 : PC44 CH1566K1B09 560P/50V_4                                             | U42 : PR231 CS41003FB32 100K<br>U42 : PC45 CH3224K1B01 0.022u/25V<br>U42 : PC40 CH3224K1B01 0.022u/25V<br>U42 : PC38 CH3224K1B01 0.022u/25V<br>U42 : PC44 CH14706KB18 470P/50V_4 |

### SVID near PU1

ZRW REV:F add 1000p

(B) H\_CPU\_SVIDDAT  
(B) VR\_SVID\_ALERTx\_VCORE  
(B) H\_CPU\_SVIDCLK

H\_PROCHOT

IMVP\_PWRGD

VRONEN

PMON

PU2  
ISL95859HRTZ-T

### Rail C

### Rail A

### Rail B

### KBL U-Line - 15W/28W

#### U22 (1+1 Phase)

**Vcore**  
Icc Max : 32A  
Icc TDC : 21A  
OCP : 38.4A

#### VCCGT

Icc Max : 31A  
Icc TDC : 18A  
OCP : 37A

#### VCCSA

Icc Max : 4.5A  
OCP : 10A

#### U42 (2+1 Phase)

**Vcore**  
Icc Max : 64A  
Icc TDC : 42A  
OCP : 76.8A

#### VCCGT

Icc Max : 28A  
Icc TDC : 12A  
OCP : 37A

#### VCCSA

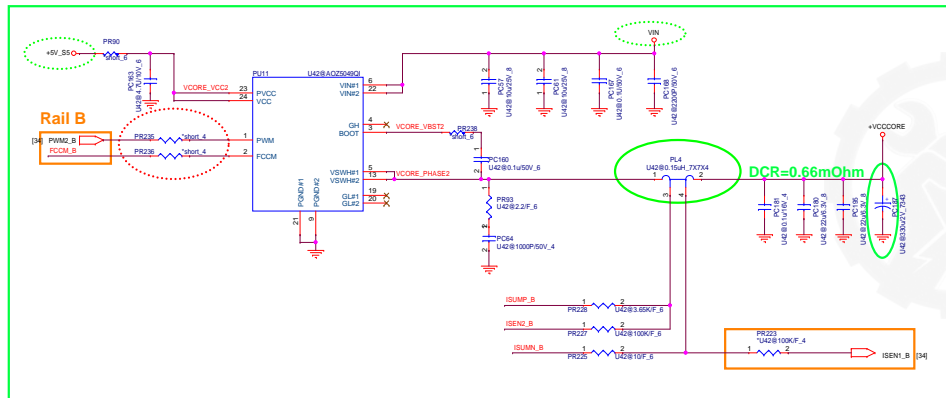
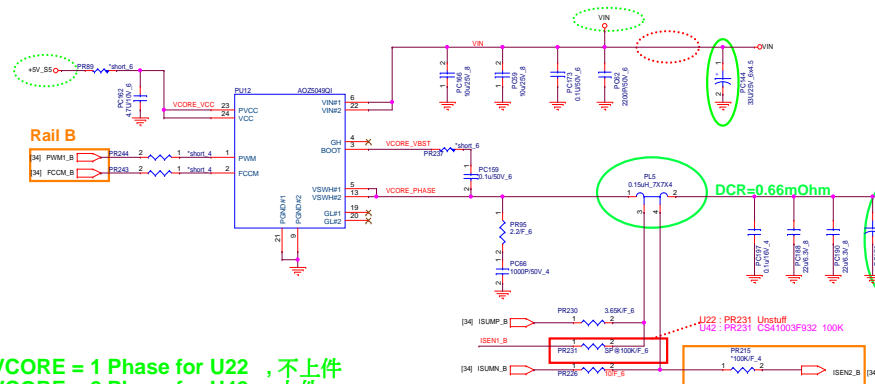
Icc Max : 5A  
OCP : 10A



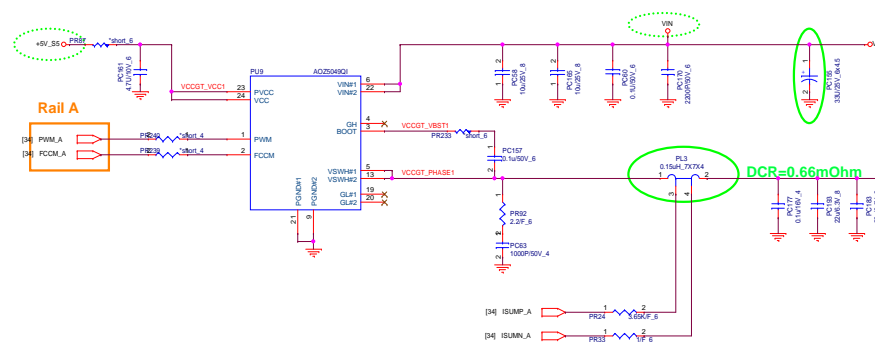
[22,25,26,30,31,32,33,34,36,37,38,39] VIN  
 [5,34] +VCCORE  
 [5,34] +VCCGT  
 [29,31,33,34,36,38,39,40] +5V\_5S

U22 : PR231 Unstuff U42 : PR231 CS41003F932 100K

## VCORE



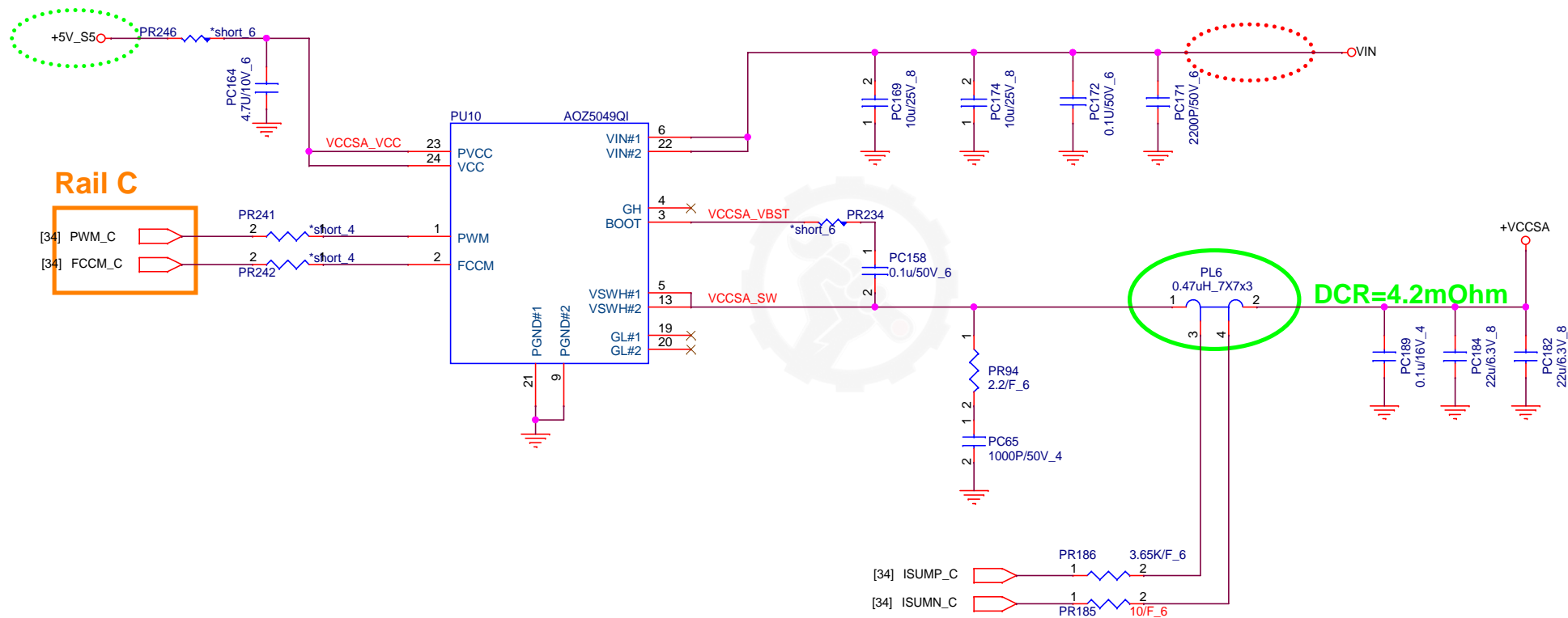
## VCCGT



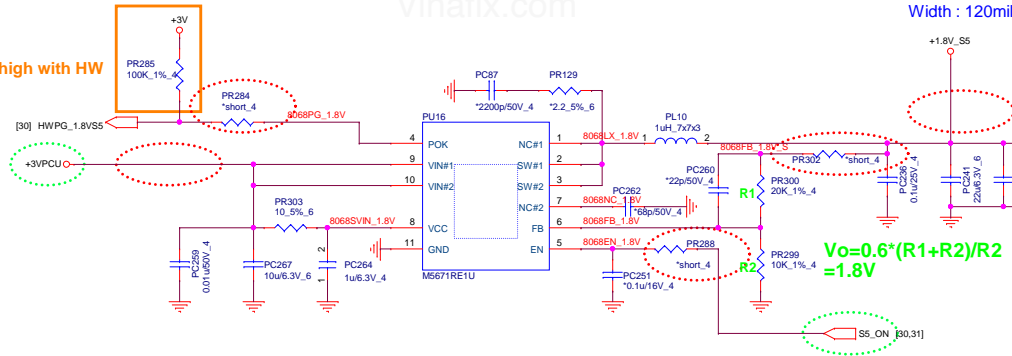
[22,25,26,30,31,32,33,34,35,37,38,39] VIN

[5,34] +VCCSA

[29,31,33,34,35,38,39,40] +5V\_S5



**Check PU high with HW**

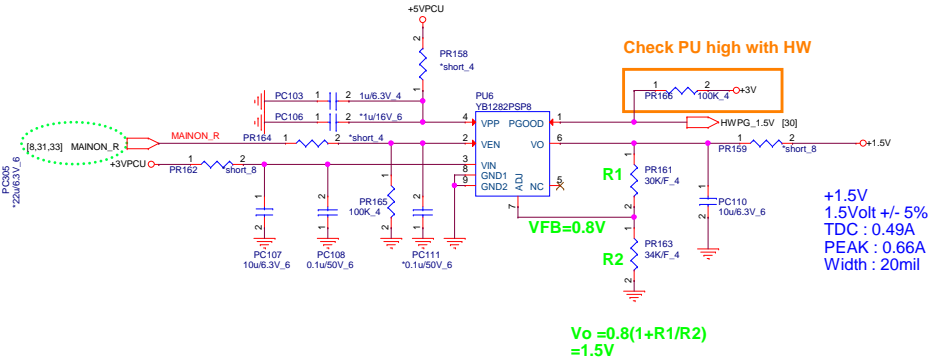


+1.8V\_S5  
1.8Volt +/- 5%  
TDC : 2.61A  
PEAK : 3.48A  
Width : 120mil

$$V_o = 0.6 \cdot (R_1 + R_2) / R_2 = 1.8V$$

S5\_ON [30,31]

Check PU high with HW

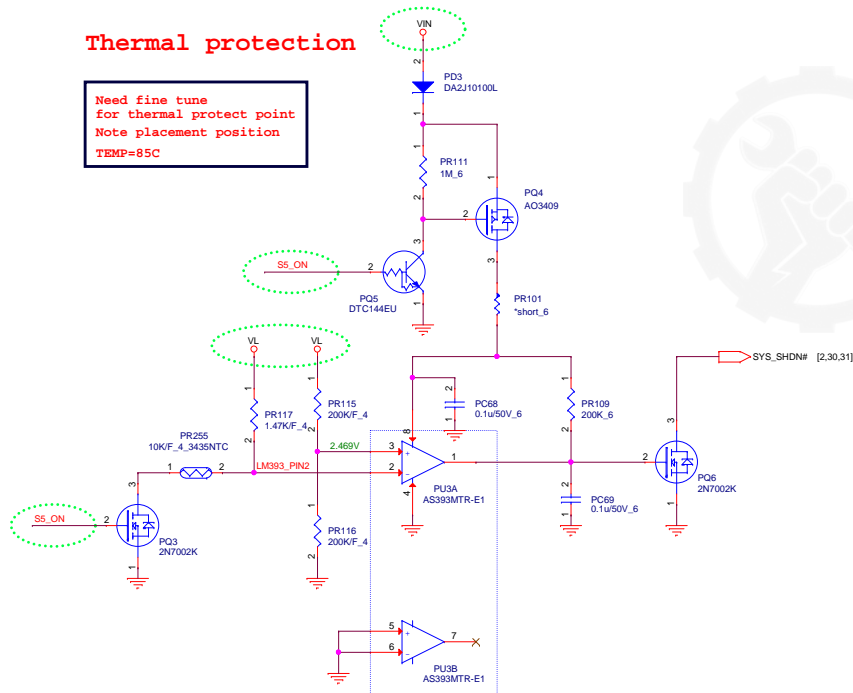


+1.5V  
1.5Volt +/- 5%  
TDC : 0.49A  
PEAK : 0.66A  
Width : 20mil

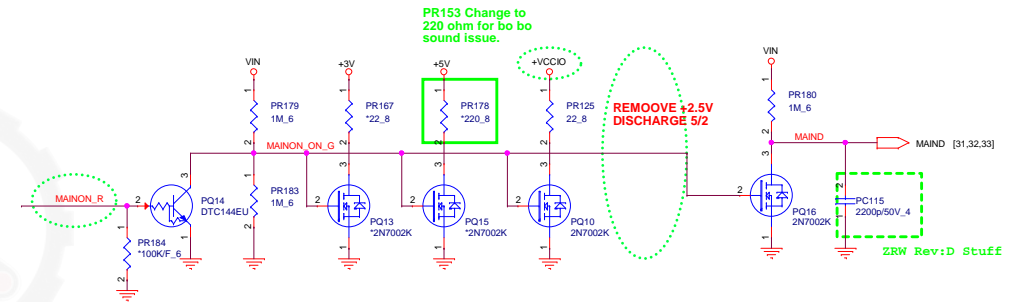
$$V_o = 0.8(1 + R_1/R_2) = 1.5V$$

## Thermal protection

Need fine tune  
for thermal protect point  
Note placement position  
TEMP=85C



For EC control thermal protection (output 3.3V)



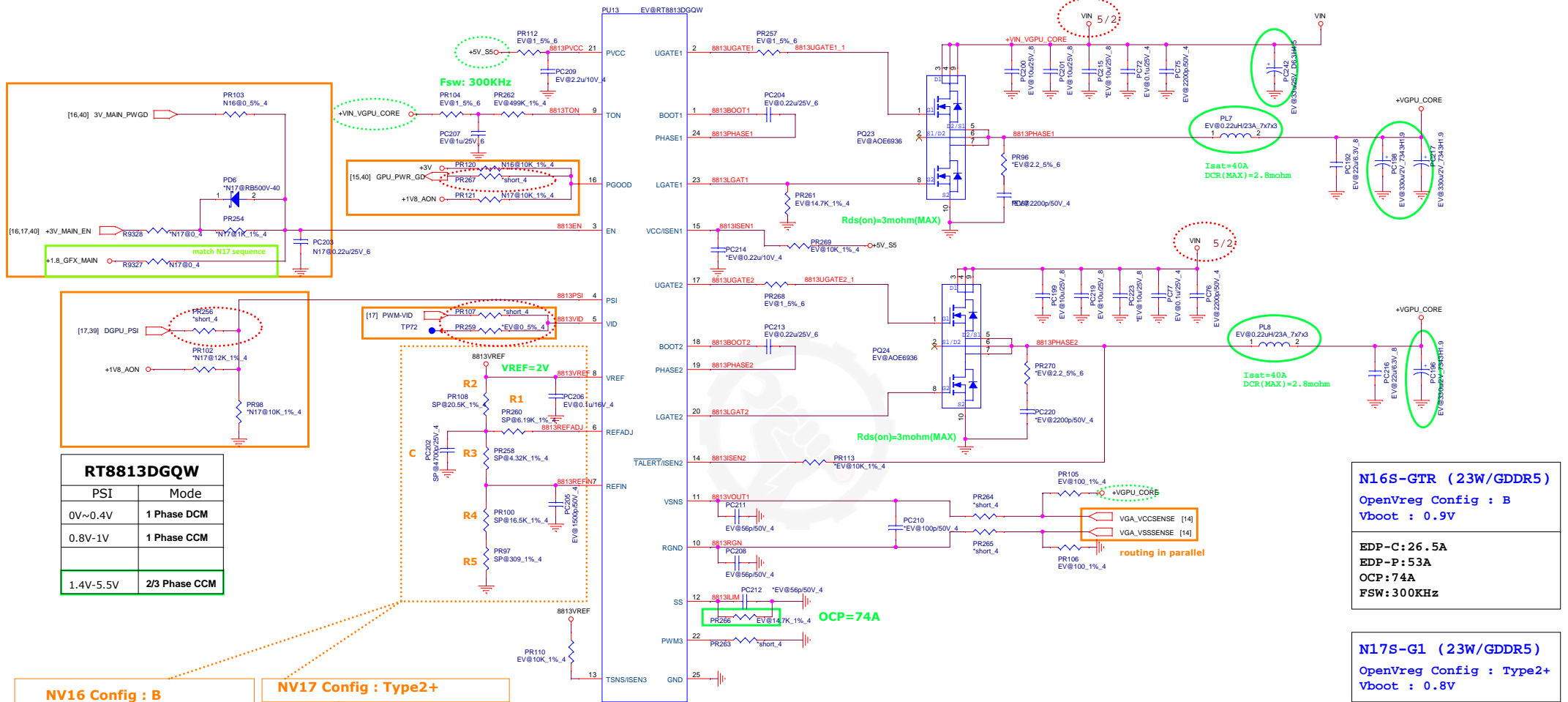
PR153 Change to 220 ohm for bo bo sound issue.

5 REMOVE +2.5V  
DISCHARGE 5/2

ZRW Rev:D Stuff

Vinafix.com

VIN [22,25,26,30,31,32,33,34,35,36,37,39]  
 +VGPU\_CORE [14]  
 +5V\_S5 [20,31,33,34,35,36,39,40]  
 +3V [2,4,5,7,8,9,12,13,14,15,16,17,20,22,23,25,26,27,28,30,31,32,33,34,37,39,40]  
 +1V8\_AON [14,16,17,39,40]



**Quanta Computer Inc.**  
**PROJECT : ZAAR**

Size Document Number  
**+NVVDD (RT8813DGQW)** Rev 1A

Date: Tuesday, June 27, 2017 Sheet 38 of 47

# 1.35V\_GFX

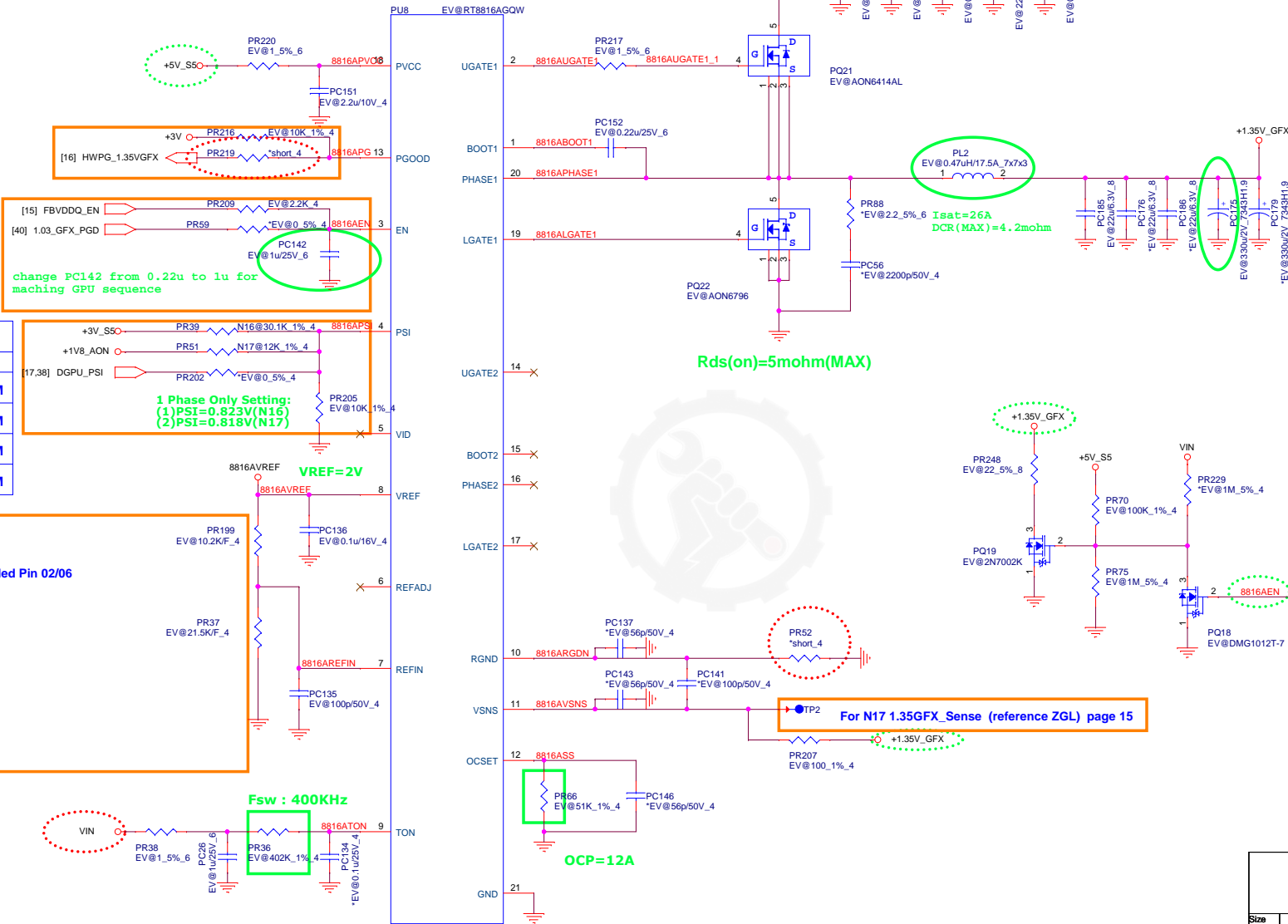
39

Vinafix.com

VIN [22,25,26,30,31,32,33,34,35,36,37,38]  
+1.35V\_GFX [15,18]  
+5V\_S5 [20,31,33,34,35,36,38,40]  
+3V\_S5 [2,3,4,6,7,8,9,11,20,23,26,27,28,30,31,33]  
+1V8\_AON [14,16,17,38,40]  
+3V [2,4,6,7,8,9,12,13,14,15,16,17,20,22,23,25,26,27,28,30,31,32,33,34,37,38,40]

| RT8816AGQW     |             |
|----------------|-------------|
| PSI            | Mode        |
| 0V to 0.4V     | 1 Phase DCM |
| 0.7V to 0.88V  | 1 Phase CCM |
| 1.08V to 1.35V | 2 Phase DCM |
| 1.6V to 5.5V   | 2 Phase CCM |

Remove N16 controlled Pin 02/06



N16S-GTR (23W/GDDR5)

OpenVreg Config : B  
Vboot : 0.9V

EDP-C:4.2A  
EDP-P:6.8A  
OCP:12A  
FSW:400KHz

N17S-G1 (23W/GDDR5)

OpenVreg Config : Type2+  
Vboot : 0.8V

EDP-C:4.6A  
EDP-P:TBD (預估TDC\*1.5=7A)  
OCP:12A  
FSW:400KHz



Quanta Computer Inc.

PROJECT : ZAAR

| Size  | Document Number          | Rev            |
|-------|--------------------------|----------------|
|       | +FBVDDQ_MEM (RT8816AGQW) | 1A             |
| Date: | Friday, June 23, 2017    | Sheet 39 of 47 |

## N16S-GTR

+3V\_GFX  
TDC : 0.06A  
Width : 20mil

## N17S-G1

+1.8V\_MAIN  
TDC : 1.13A  
PEAK : 1.5A  
Width : 60mil

## N17S-G1

+1.8V\_AON  
TDC : 1.13A  
PEAK : 1.5A  
Width : 60mil

PR99 For N17  
use only

A2

Check N16 Power Good

Check PU high with HW

|      | R1      | R2      |
|------|---------|---------|
| N16S | 133 ohm | 124 ohm |
| N17S | 133 ohm | 124 ohm |

| N16S-GTR                                             | N17S-G1                                           |
|------------------------------------------------------|---------------------------------------------------|
| +1.05V<br>TDC : 0.8A<br>PEAK : 2.1A<br>Width : 80mil | +1V<br>TDC : 0.9A<br>PEAK : 1.1A<br>Width : 40mil |

$$N16S:Vo = (1+R1/R2) * 0.5 = 1.03V$$

$$N17S:Vo = (1+R1/R2) * 0.5 = 1.03V$$



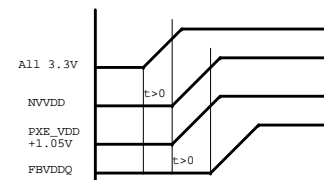
The diagram illustrates the power management system for the SKYLAKE PCH, showing the +3V\_CPU and +3V\_MAIN power rails. The system includes MOSFETs, PWMs, OR gates, and various control signals.

**Power Rails and Components:**

- +3V\_CPU:** Input to the first MOSFET.
- +3V\_GFX:** Output of the first MOSFET, input to the second MOSFET.
- +3V\_MAIN:** Output of the second MOSFET.
- MOSFETs:** Two MOSFETs are shown, controlling the power rails.
- PWMs:** Two PWMs are shown, controlling the power rails.
- OR Gate:** An OR gate is shown, combining signals from the PWMs and the EC.

**Control Signals and Connections:**

- DGPU\_PWR\_EN:** Input to the first MOSFET.
- 3V\_MAIN\_EN (GPU GPIO5):** Input to the second MOSFET.
- 3V\_MAIN\_PWGD:** Output of the second MOSFET, input to the first MOSFET.
- PWM-VID (GPU GPIO11):** Input to the first PWM.
- VIN:** Input to the first PWM.
- 3V\_MAIN\_PWGD:** Input to the first PWM.
- VGPU\_PWRGD:** Output of the first PWM, input to the OR gate.
- EC\_FB\_CLAMP (EC):** Input to the OR gate.
- GC6\_FB\_EN (GPU GPIO0):** Input to the OR gate.
- FBVDDQ\_EN:** Output of the OR gate, input to the second PWM.
- HWPG 1.5VGFX:** Input to the second PWM.
- VGPU\_PWRGD:** Input to the second PWM.
- DGPU\_PWROK:** Output of the second PWM.



N15x Power on sequence

Notes: -All 3.3V includes all rails powered at 3.3V  
-PEX\_VDD 1.05V includes all rails that are shared

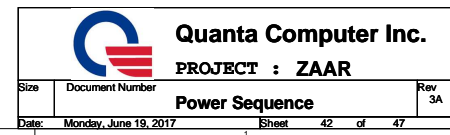
I/O 3.3V

PEX\_RST

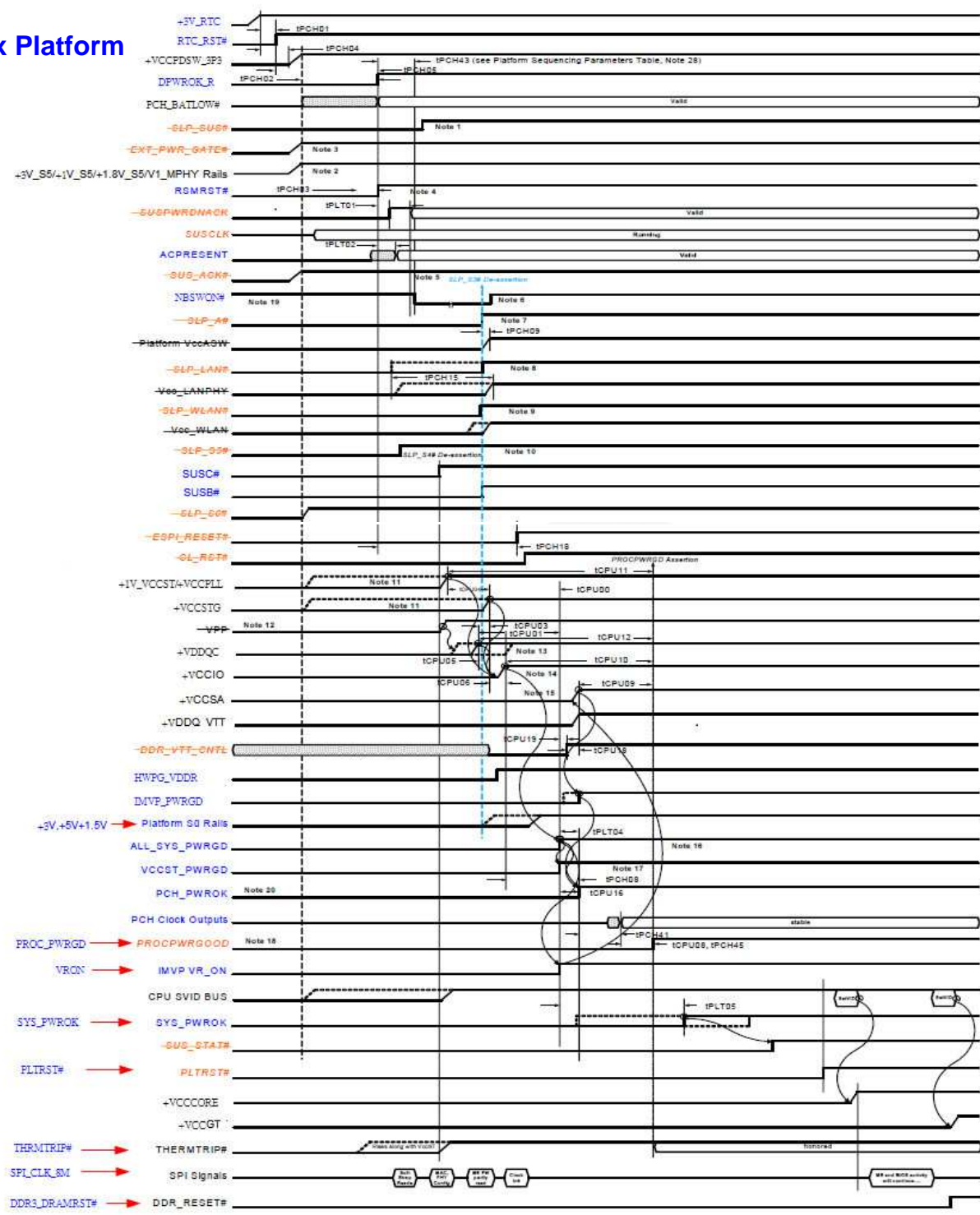
$T_{rise} \geq 1\mu S$

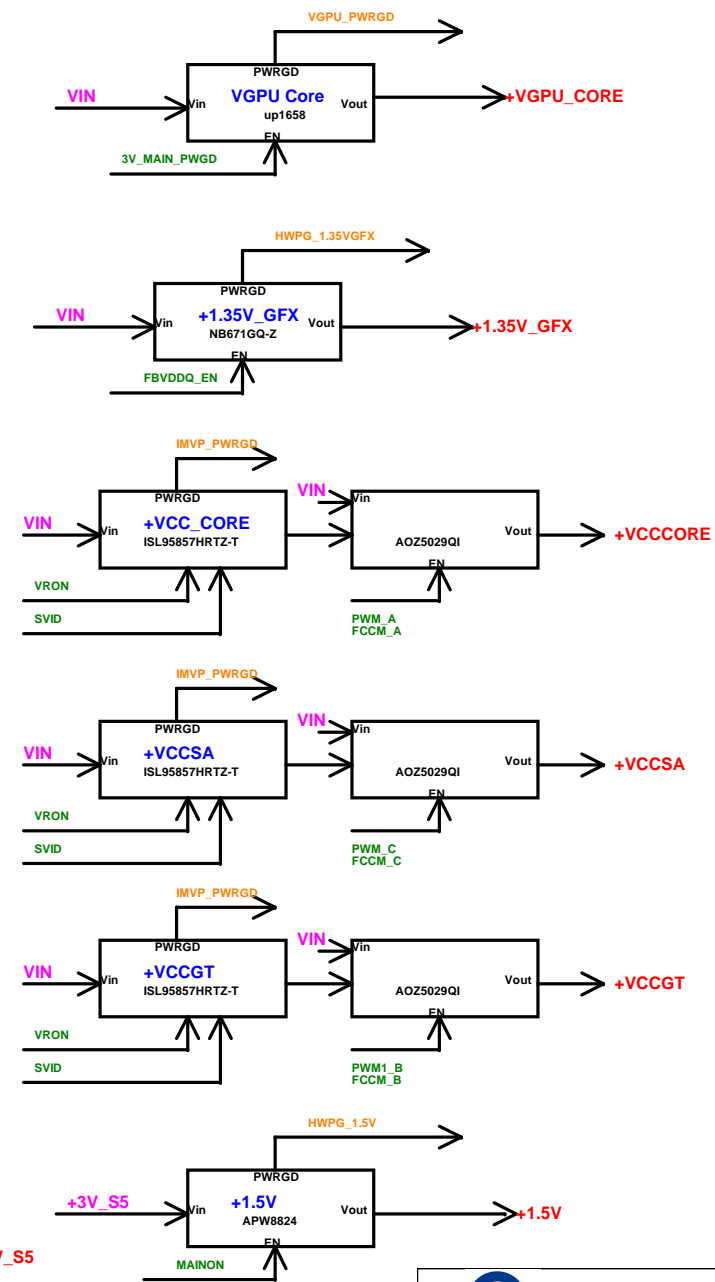
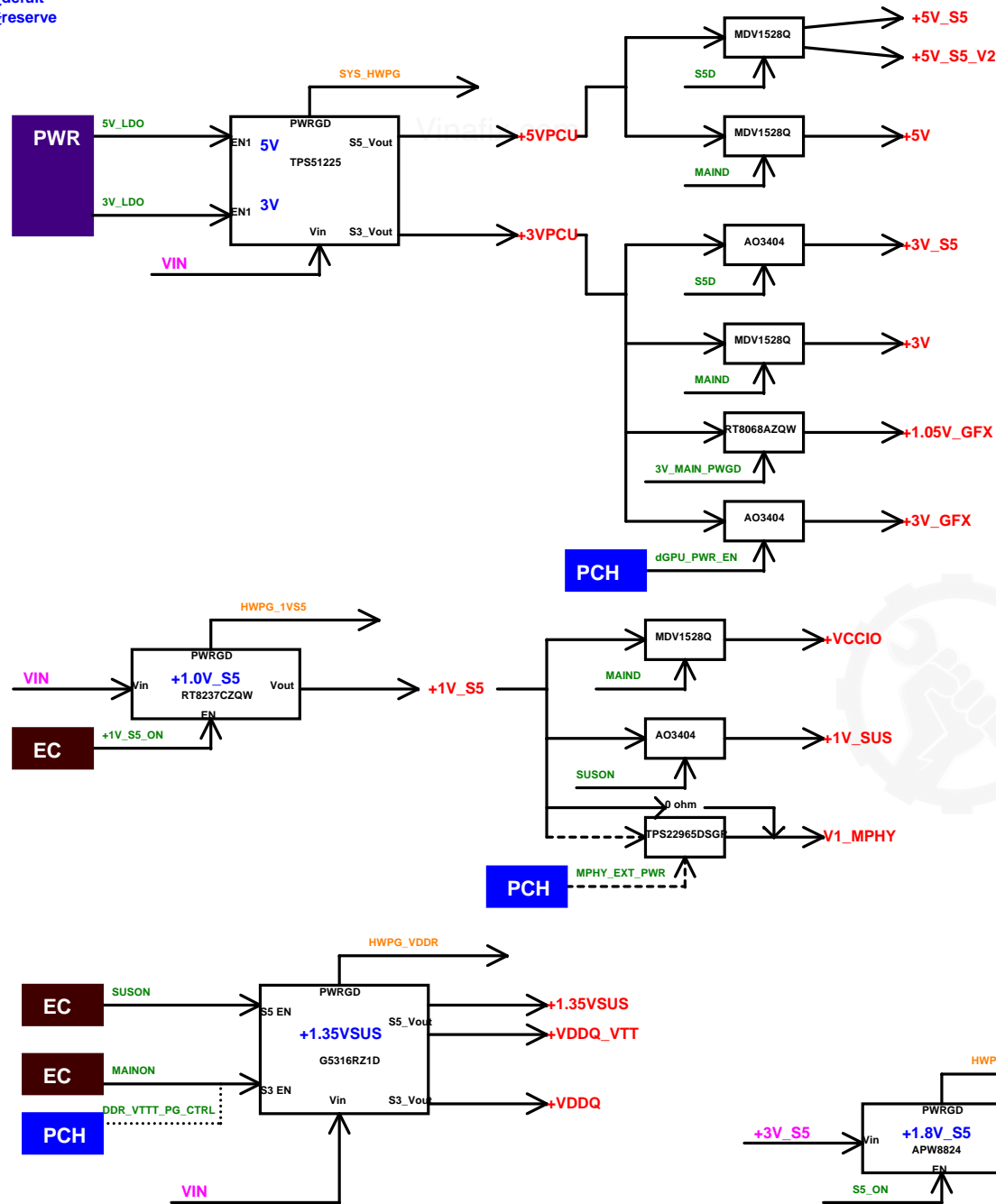
$T_{fall} \leq 500ns$

## Non Deep Sx

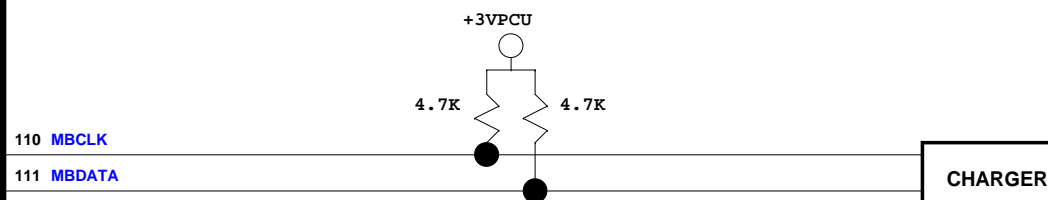
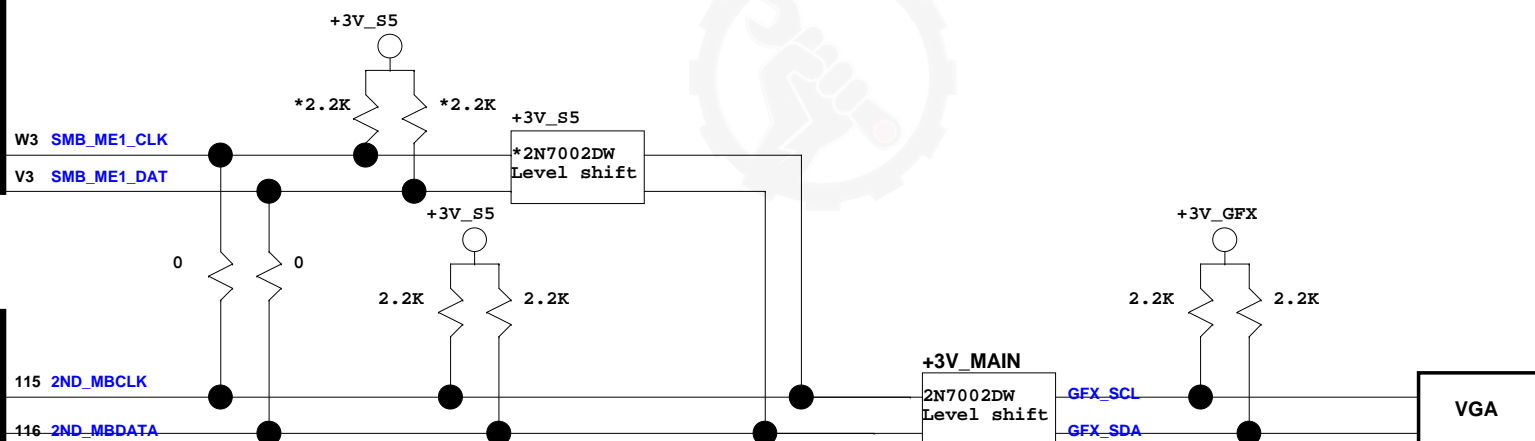
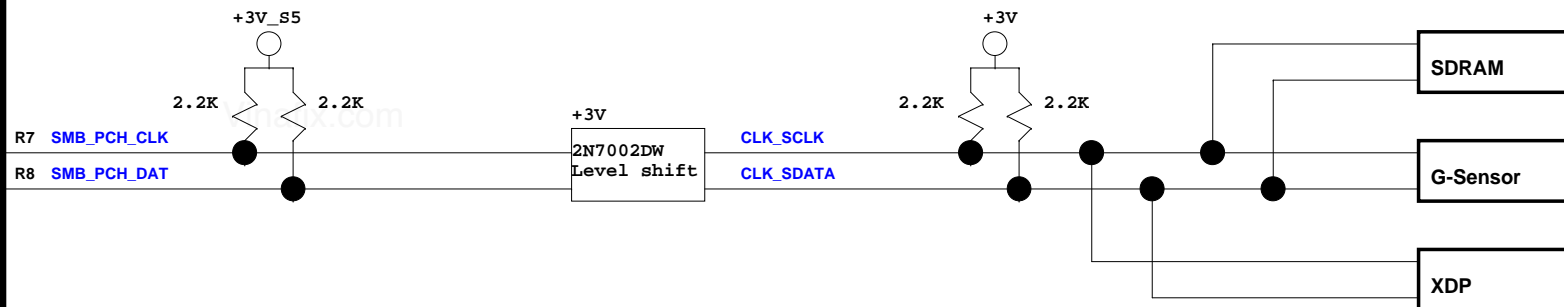


Skylake U Non-Deep Sx Platform  
Power on sequence






Skylake U



| Stage | Date  | CHANGE LIST                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A     | 02/02 | 1. change C8773 C8774 C8775 C8776 C8777 form 1u to 10u ( page 5 )<br>2.Pin V20&V21 add C8779 & C8780 22u follow ZAV ( page 9 )<br>3.Change R1 from 100 ohm to 133 ohm and Change R2 from 100 ohm to 124 for 1.03V ( page 40 )                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|       | 02/06 | 1. change net 1.35GFX_Sense to TP8070 (reference ZGL page 15 ) page 39<br>2. change R536 value from 1M_4 to U22@1M_4 page 6<br>3. change Y4 value from 24MHz to U22@24MHz page 6<br>4.Add Q8030 & Q8031 level shift circuit for N17 page 17<br>5. GPU ball C1 is define to STRAP5 for N17S GPU ,PU R11314 and PU R11315 page 17<br>6. Add D4015 for GPU_EVENT# suggest to use backdrive diode page 17<br>7. add +1V8_AON R11311 for N17 and +3V_GFX R11312 for N16 page 17<br>8. change Q8028 from DTC144EUA to PJA138K page 16<br>9. Remove N16 controlled Pin SCH and change PR9049 from 10k to 10.2k, change PR9052 from 30.1k to 21.5k page 39<br>10. Remove R8293 and net MEM_VDD_CTRL page 17<br>11. R740 & R382 change powr from +3V_GFX to +3V page 29<br>12. remove R8297 page 15<br>13. R45change powr from +3V_GFX to +3V page 17<br>14. Add R11316 for N17 page 16<br>15. L03_GFX_PGD en 1.35V_GFX page 39 40<br>16. Stuff R204 page 4 |
|       | 02/07 | 1. Change PC9092 from 0201(1u) to 0402 (1u ) page 37<br>2. Add FJ9024 at Vin (VCCSA) page 36<br>3. Change R8264 power from +3V-GFX to +3V page 17<br>4. Change Q8017 power from +3V_GFX to DGPU_PWROK page 14<br>5.Change Q129 to PJA138K page 18<br>6. Remove R8352 page 17<br>7. Remove PQ40 page 30<br>8.Add R11317 and R11318 at Q8022 Pin2 page 17<br>9. U9 Pin 12 connect EC_TypeC_EN_R ( unstuff R11319 ) page 19<br>10. Change U8018 from MC74VHC1G08DFT2G to NL17SZ08DFT2G and add R11320 for N16 POWER & R11321 for N17 POWER page 14<br>11. Change Q8017 from source to net page 14<br>12. Change PR9076 , PR9044 , PR9009 , PR9018 form +1.8V_AON to +1V8_AON page 38,39,40                                                                                                                                                                                                                                                            |
|       | 02/08 | 1. Update N17 & N16 STRAP pin & ROM pin page 17                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|       | 02/09 | 1.GPU ball A7 & B7 reserve 1.8K pull up to +1V8_AON power rial for N17S GPU page 16<br>2. Unstuff R8337 for N17S GPUpage 17<br>3. Remove R8353 is ok both for N16S and N17S GPU. page 17<br>4.Connect R8349 to +1V8_AON power rail for N17S GPU page 17<br>5. Connect R8682,R8679,R8676 and R8675 to +1V8_AON for N17 S GPU page 17<br>6. add GPIO5 (net name is +3V_MAIN_EN) for N16S GPU page 17<br>7.Both GPU and VRAM side have have pull up and pull down resistors. Please remove either one is ok page15<br>8.Remove C8745 page3<br>9.RAM_ID1 for U22 or U42 & Board_ID7 for ZAAR page8                                                                                                                                                                                                                                                                                                                                                     |
|       | 02/10 | 1.Add PR67000 page 39<br>2.Remove GND ( 8813RGN ) page 38<br>3.Add PR67001 page 40<br>4.Remove R8263 page 15                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| B2    | 02/11 | 1.Add C9093 page 30<br>2.Reserve D4016 page 22<br>3.Double check R781 from 20k ohm to 10k ohm ??? ( keep 20k , PDG 10k )<br>4.Reserve C750 page 3<br>5.Unstuff C696 base on ZBV ( 47u * 6 ) page 5<br>6.Stuff R631 base on PDG page 6<br>7.Change pull up ( IRQ_SERIRQ ) from +3V to +3V_S5 base on Z8V page 7 ( but PDG connect +3V )<br>8. Add ESD7 and ESD6 page 22                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|       |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

|                                                                                    |                 |                   |  |         |                 |      |              |            |           |            |
|------------------------------------------------------------------------------------|-----------------|-------------------|--|---------|-----------------|------|--------------|------------|-----------|------------|
|  |                 | PROJECT : ZAAR    |  | DOC NO. | PROJECT MODEL : | ZAAR | APPROVED BY: | JC Huang   | DATE:     | 2016/04/13 |
| File                                                                               | Document Number | Change list - 1/2 |  | Rev     | PART NUMBER:    |      | DRAWING BY:  | Dennis Lin | REVISION: | 3A         |
| Date: Monday, June 13, 2017                                                        |                 | From: ss          |  | at: 47  |                 |      |              |            |           |            |



|                                                                                                                                                                                                                                                                                                                                                                      |         |                 |      |              |            |           |            |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|-----------------|------|--------------|------------|-----------|------------|
|  <b>Quanta Computer Inc.</b><br><b>PROJECT : ZAAR</b><br><div> <div>Rev</div> <div>Document Number</div> <div>1A</div> </div> <b>Change list - 2/2</b><br><div> <div>Date</div> <div>Monday, June 13, 2017</div> <div>Drawn</div> <div>42</div> <div>of</div> <div>42</div> </div> | DOC NO. | PROJECT MODEL : | ZAAR | APPROVED BY: | JC Huang   | DATE:     | 2016/04/13 |
|                                                                                                                                                                                                                                                                                                                                                                      |         | PART NUMBER:    |      | DRAWING BY:  | Dennis Lin | REVISION: | 3A         |